

Compal Confidential

MB Schematic Document

GH51G/GH71G/GH53G/GH57G/GH73G

LA-L181P

Rev:1A

2021.03.18

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	Cover Sheet
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USB3 Re-driver
- PS8713

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Vcc	3.3V +/- 5%	EC Board ID Table for AD channel			
Ra	100K +/- 1%				
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

	*PCB Version *Key board type
Board ID	PCB Revision
0	50 Rev0.1
1	50 Rev0.2
2	50 Rev1.0
3	
4	50 Rev0.1+RGB
5	50 Rev0.2+RGB
6	50 Rev1.0+RGB
7	
8	60 Rev0.1
9	60 Rev0.2
10	60 Rev1.0
11	
12	60 Rev0.1+RGB
13	60 Rev0.2+RGB
14	60 Rev1.0+RGB
15	
16	
17	
18	
19	

SIGNAL	SLP_S#3	SLP_S#4	SLP_S#5	+VALW	+V	+VS
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDBGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDBGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+FBVDDQ	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+PEXVDD	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_1 (+3VALW)	TM-P3393-003 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1,DIMM2			
PCH_SML0CLK(1.8VALW)	BBR1,BBR2			
PCH_SML1CLK(1.8VALW)	PD TPS65991			
EC_SMB_CK0(+3VLP_EC)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
	N18P-G61-A/GN20P (VGA)	0x9E		
EC_SMB_CK1(+3VLP_EC)	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	Thermal Sensor (G781)	1001_101xb	1001_1011b	1001_1010b
EC_SMB_CK2(+5VS)	LED driver	0xC0		
EC_I2C_3_SCL (+3V_TBTA_PDLDO)	PD TPS65991	0x21		
I2C3_PD_R_CLK (+3V_TBTA_PDLDO)	BBR1	0x53		
	BBR2	0x54		
Reserved	KC3810	Reserved		

Item (X43 / X76)	BOM Structure	Item (X43 / X76)	BOM Structure
Unpop	@	eDP-TS USB	TS_USB@
Connector	CONN@	eDP-TS I2C	TS_I2C@
PCB	PCB@	mDP	DP@
UMA Only(Reserved)	UMA@	TypeC	TypeC@
TGL ES PCH	QVTB@	Intel CNVI	CNVI@
		For UART debug	UART@
TGL ES CPU	QWCC@	Extend GPIO	KC3810@
	QWCB@		NKC3810@
		KB LED driver	LED14P@
		PERKEY KB	PERKEY@
TGL ES sample	ES@	Finger Print	FP@
TGL QS sample	QS@	TPM pop	TPM@
CMC	CMC@		2LD@
		TPM non-pop	1LD@
dGPU circuit	VGA@	Power sequence	VOL@
N18P-G61-A	N18PA@		PREM@
N20P	N20P@	SPI ROM 16MB	16MB@
OVRM	OVRM@	SPI ROM 32MB	32MB@
OVRM GEN1	GEN1@	5V_FAN	5VFAN@
OVRM GEN2	GEN2@	12V_FAN	12VFAN@
ON GEN1	ON_GEN1@	Thermal sensor	TMS@
UPI GEN1	UPI_GEN1@		
ON GEN2	ON_GEN2@	Debug SW	EVT@
UPI GEN2	UPI_GEN2@	EC board ID	NONRGB@
			RGB@

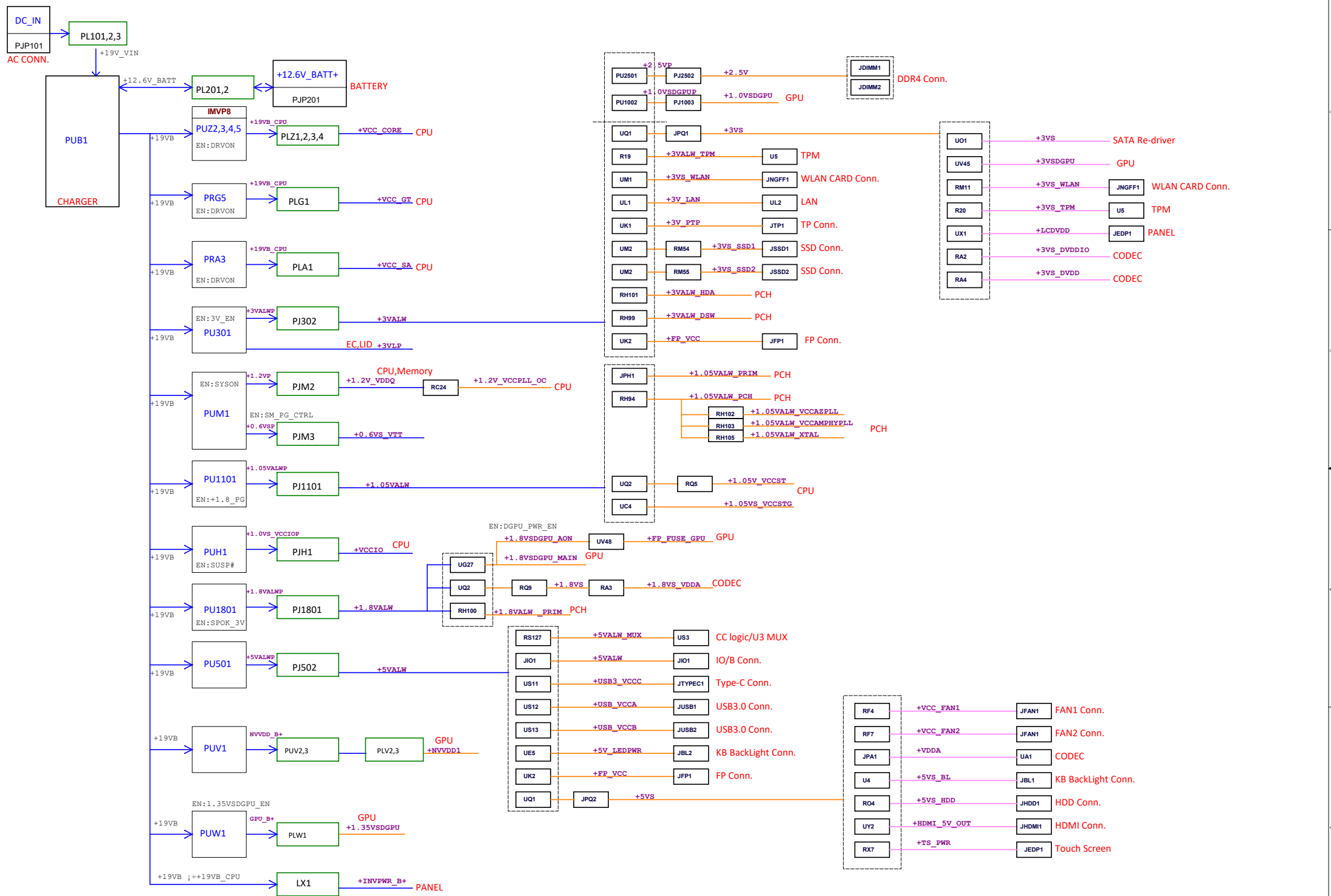
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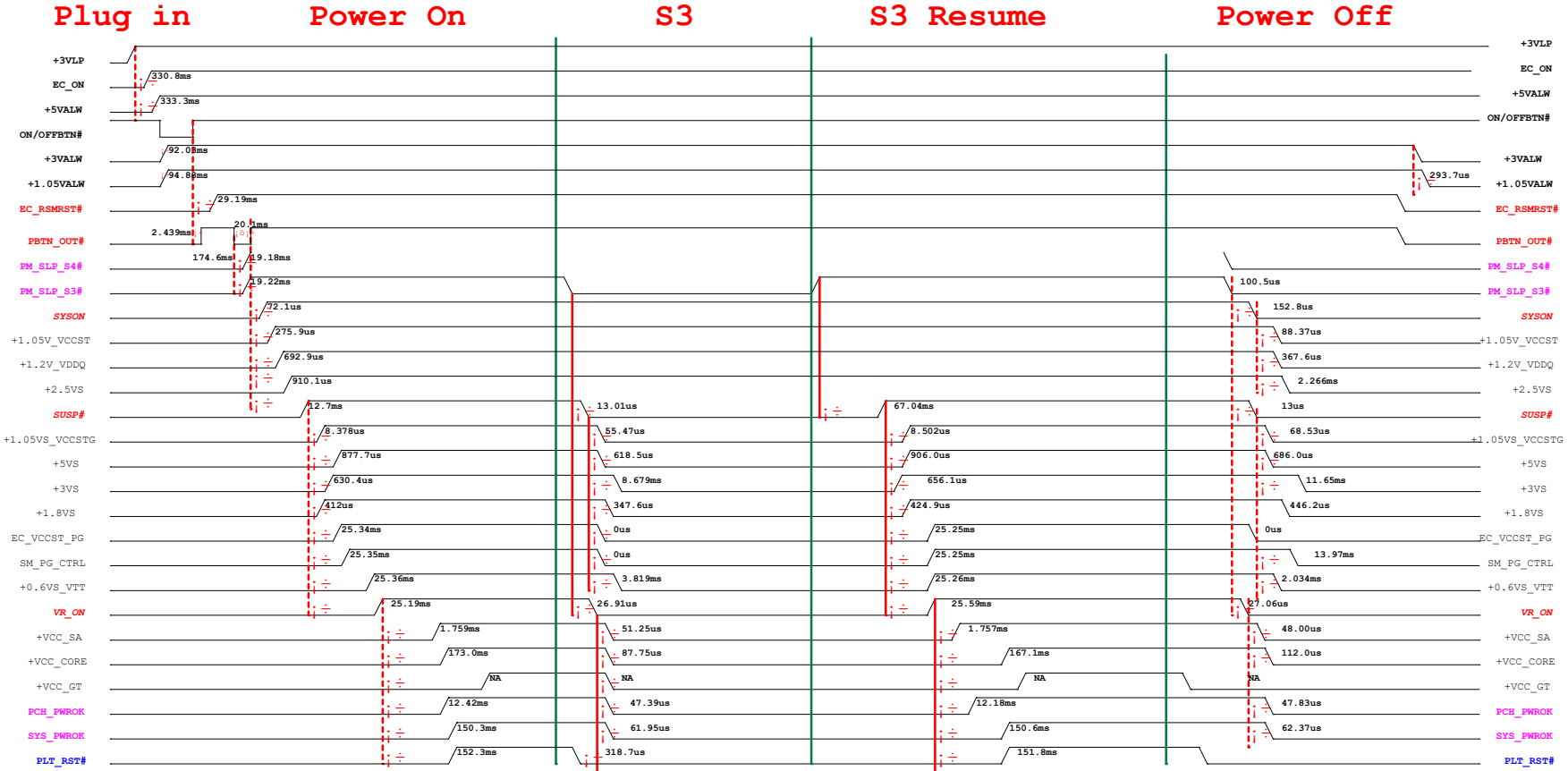
Item (X4E)	BOM Structure
EMI requirement	EMI@ ∇
EMI require reserve	XEMI@
ESD requirement	ESD@ ∇
ESD require reserve	XESD@
FP ESD requirement	FPESD@ ∇
RF requirement	RF@ ∇
RF require reserve	XRF@
X4E	EMC for EE

Item (X76)	BOM Structure
OVRM-uPI	uPI_X76@
OVRM-ON	ON_X76@
VRAM-SAMSUNG	X76SAM@
VRAM-MICRON	X76MIC@

```
X76869BOL01 - MICRON
X76869BOL02 - SAMSUNG
X76869BOL03 - ON OVRM
X76869BOL04 - UPI OVRM
```

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PCB GH51G LA-L181P LS-K851P/K852P/K853P
DAZ31Z00101

CPU

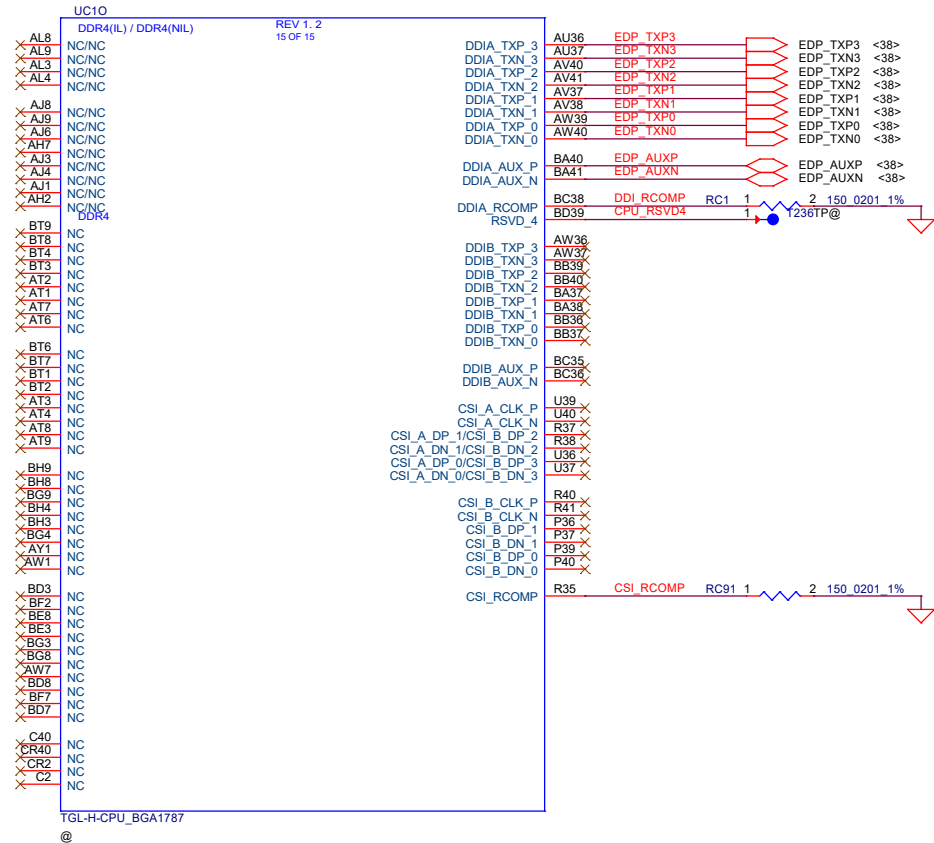
UC1 SRKT0@
S IC FH8069004351513 SRKT0 R0 2.6G ABO !
SA0000EFE20

UC1 SRKT1@
S IC FH8069004351613 SRKT1 R0 2.7G ABO !
SA0000EDJ30

UC1 SRKT3@
S IC FH8069004352018 SRKT3 R0 2.3G ABO !
SA0000EDK30

PCH

UH1 SRKMA@
S IC FH82HM570 SRKMA B1 FCBGA 943P ABO !
SA0000EDM60



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Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	TGL-H(1/8)DDI/CSI/Memory
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Type-C Port0



+1.05VS_VCCSTG

RC380
1K_0201_5%

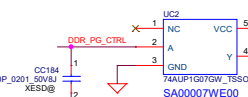
CPU_EAR#

RC86
1K_0201_5%
@

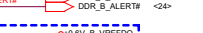
Singal : CPU_EAR#
Usage : Stall reset sequence after PCU PLL lock until de-asserted:
LOW : Stall
HIGH : (Default) Normal Operation; No stall.

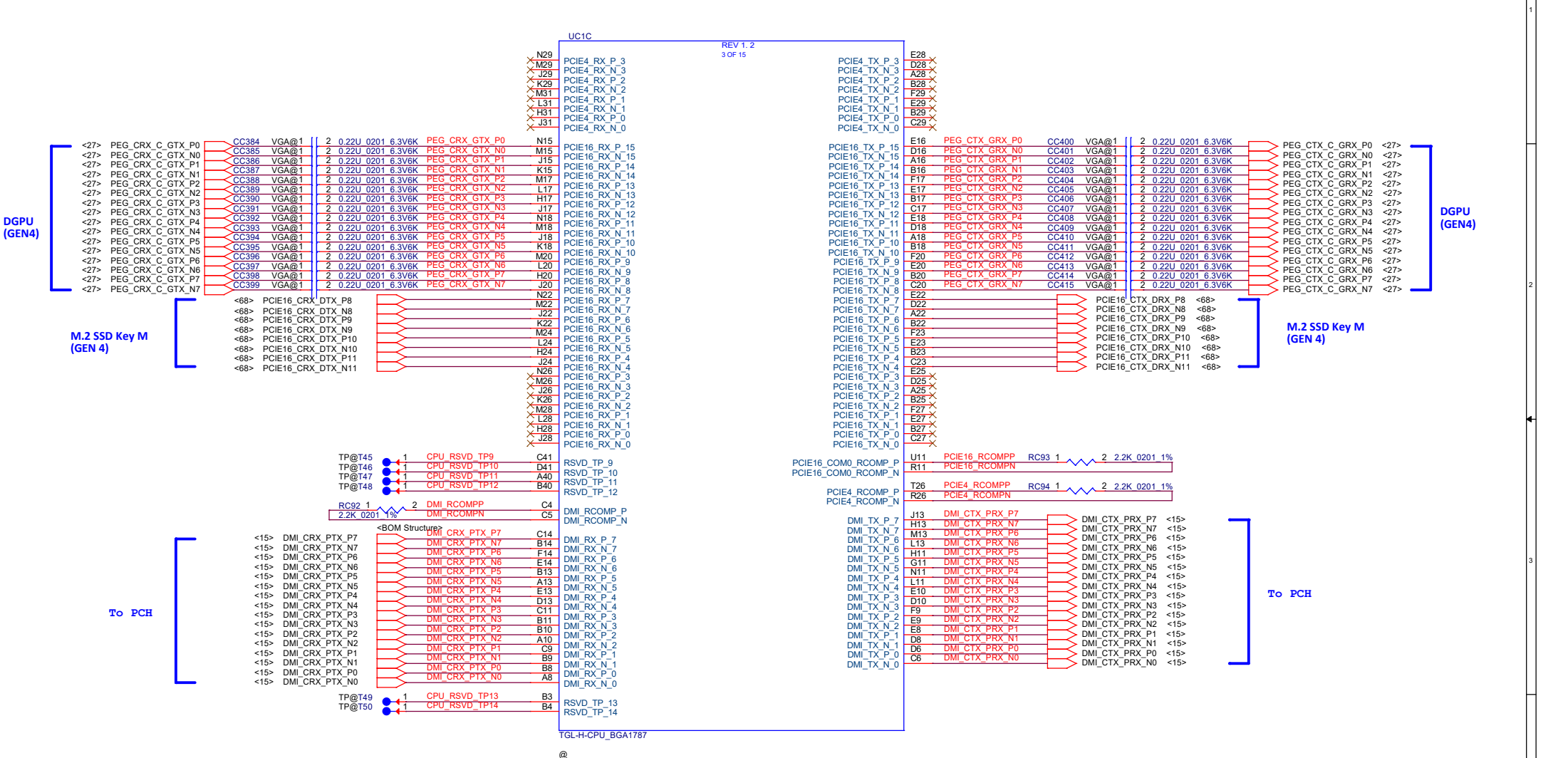
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Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	TGL-H(2/8)TCP/DPIP
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Interleaved Memory



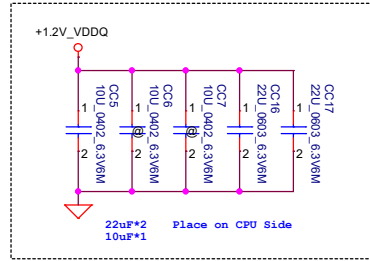
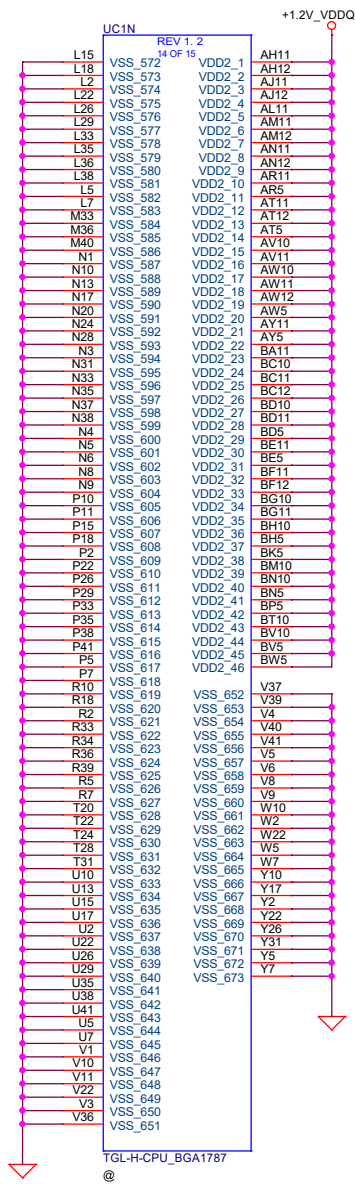
Interleaved Memory



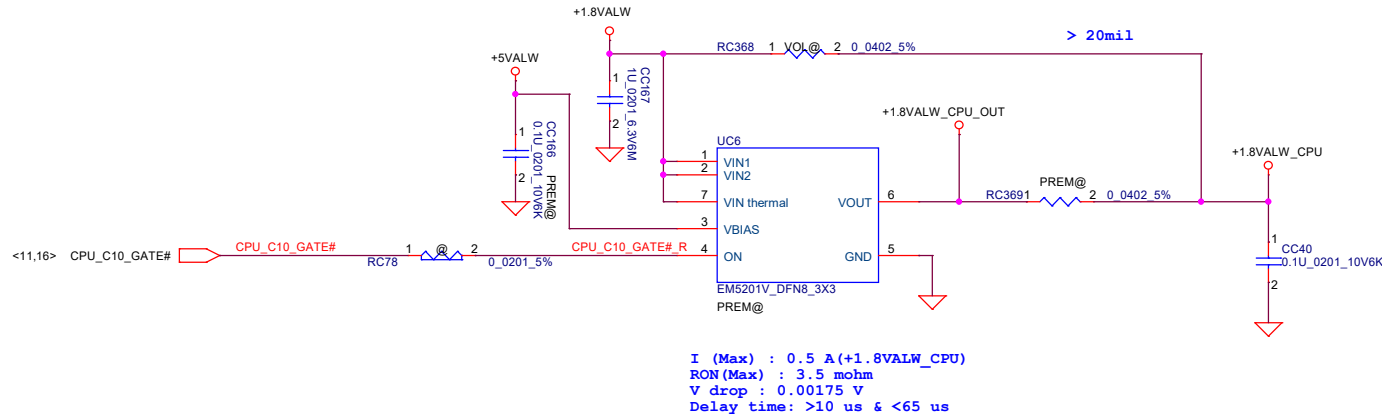
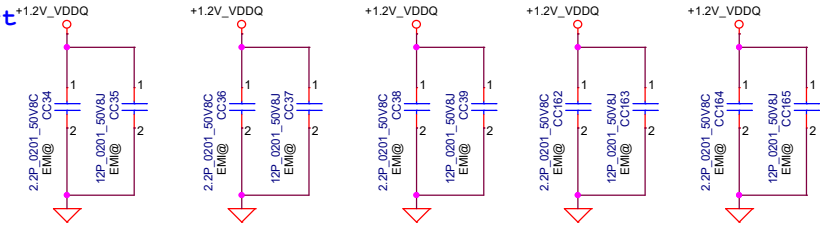


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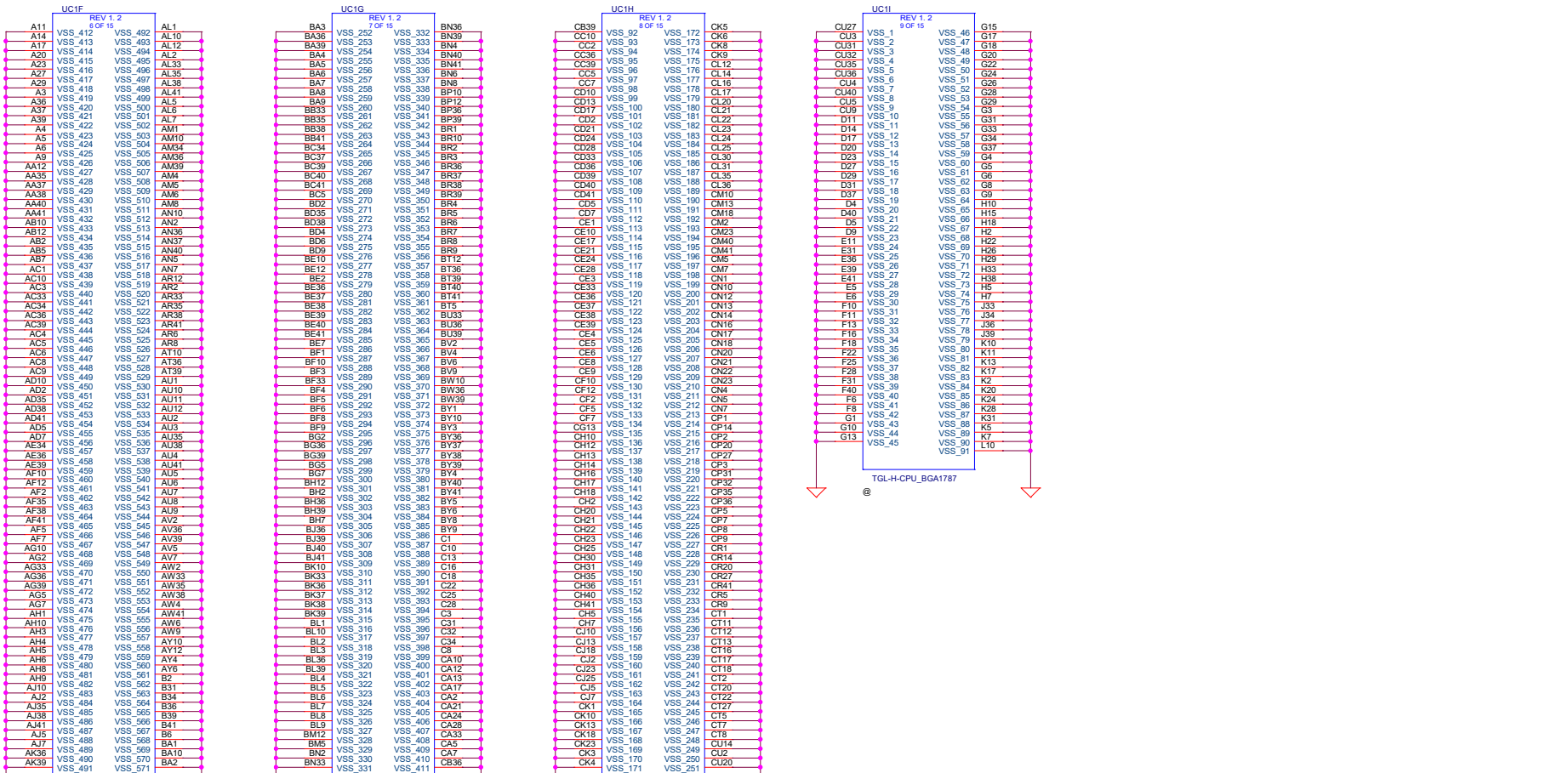




EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



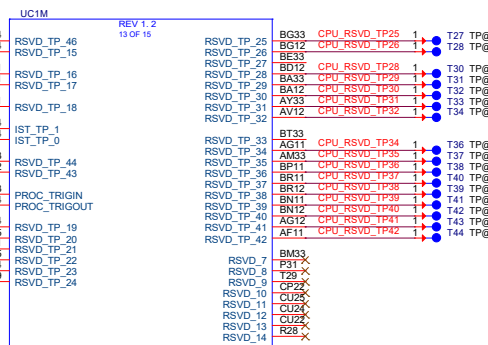
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	TGL-H(7/8)Power,VCCIN AUX/VDDQ
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<19> PCH_TRIGOUT
<19> CPU_TRIGOUT

PCH_TRIGOUT
CPU_TRIGOUT

TP@ T20 1 CPU_RSVD_TP19 CN24
TP@ T21 1 CPU_RSVD_TP20 CN25
TP@ T22 1 CPU_RSVD_TP21 CN26
TP@ T24 1 CPU_RSVD_TP23 CN24
TP@ T25 1 CPU_RSVD_TP24 R25



PCH_CPU_NSSC_CLK_N_R RH366 1 ES@ 2 0 0201 5% PCH_CPU_NSSC_CLK_P
PCH_CPU_NSSC_CLK_P_R RH365 1 ES@ 2 0 0201 5% PCH_CPU_NSSC_CLK_N

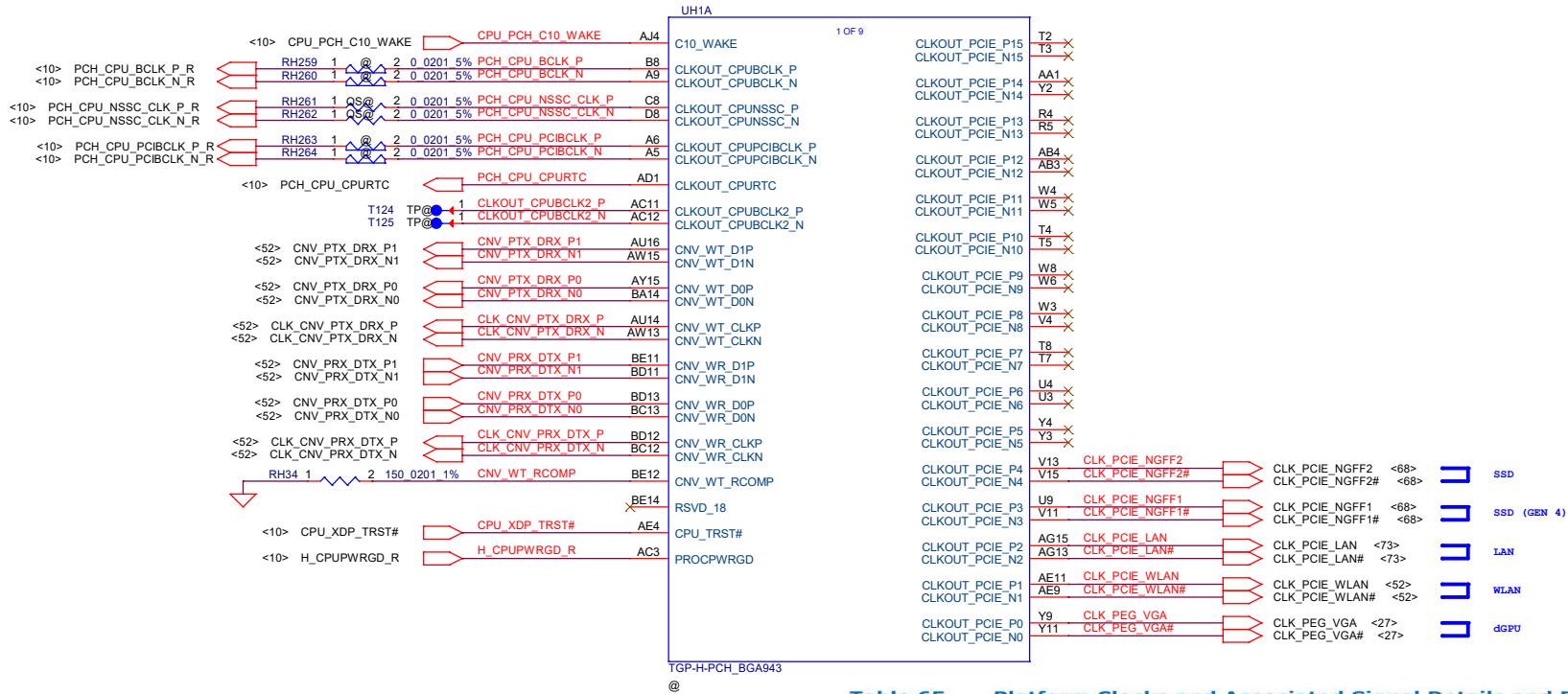
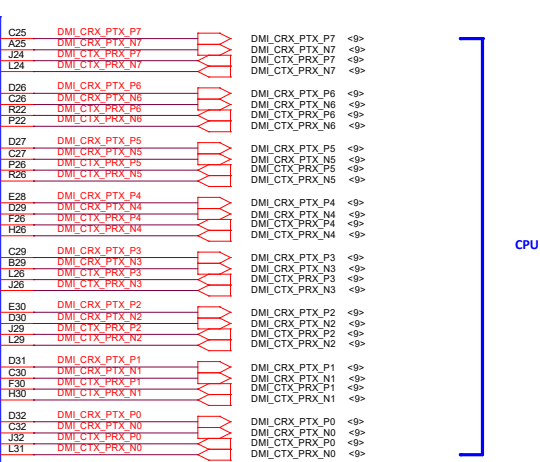
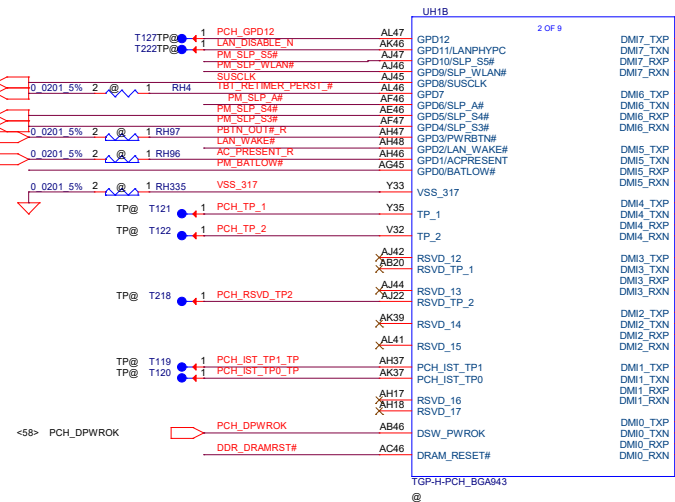
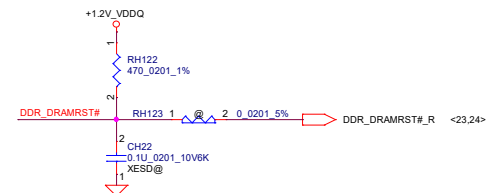
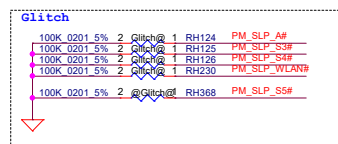
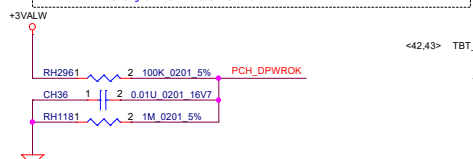
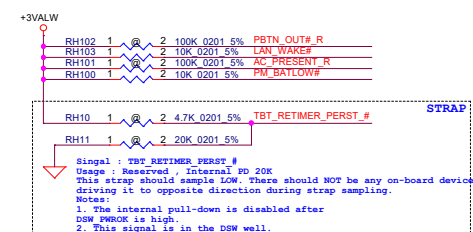


Table 65. Platform Clocks and Associated Signal Details and Descriptions

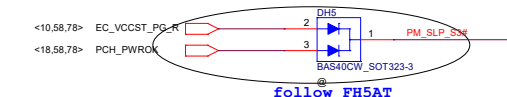
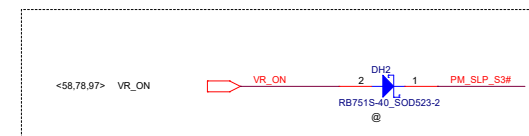
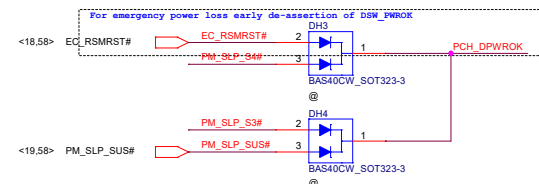
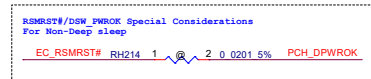
Signal Name	Type	SSC Capable	Description
CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC_N	O	No	Filtered Crystal Reference Clock to CPU: 24MHz differential, filtered crystal reference clock to the processor
CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK_N	O	Yes	Differential Clock to CPU: Reference clock to the processor 100-MHz differential core
CLKOUT_CPUPCIBCLK_P CLKOUT_CPUPCIBCLK_N	O	Yes	Differential PCIe* Reference Clock to CPU: 100-MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	PCI Express* Clock Output: PCI Express* Clock Output; Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices. <ul style="list-style-type: none">CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 supportCLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

continued...

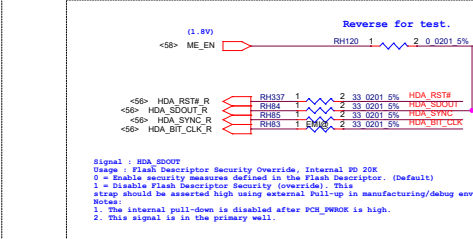
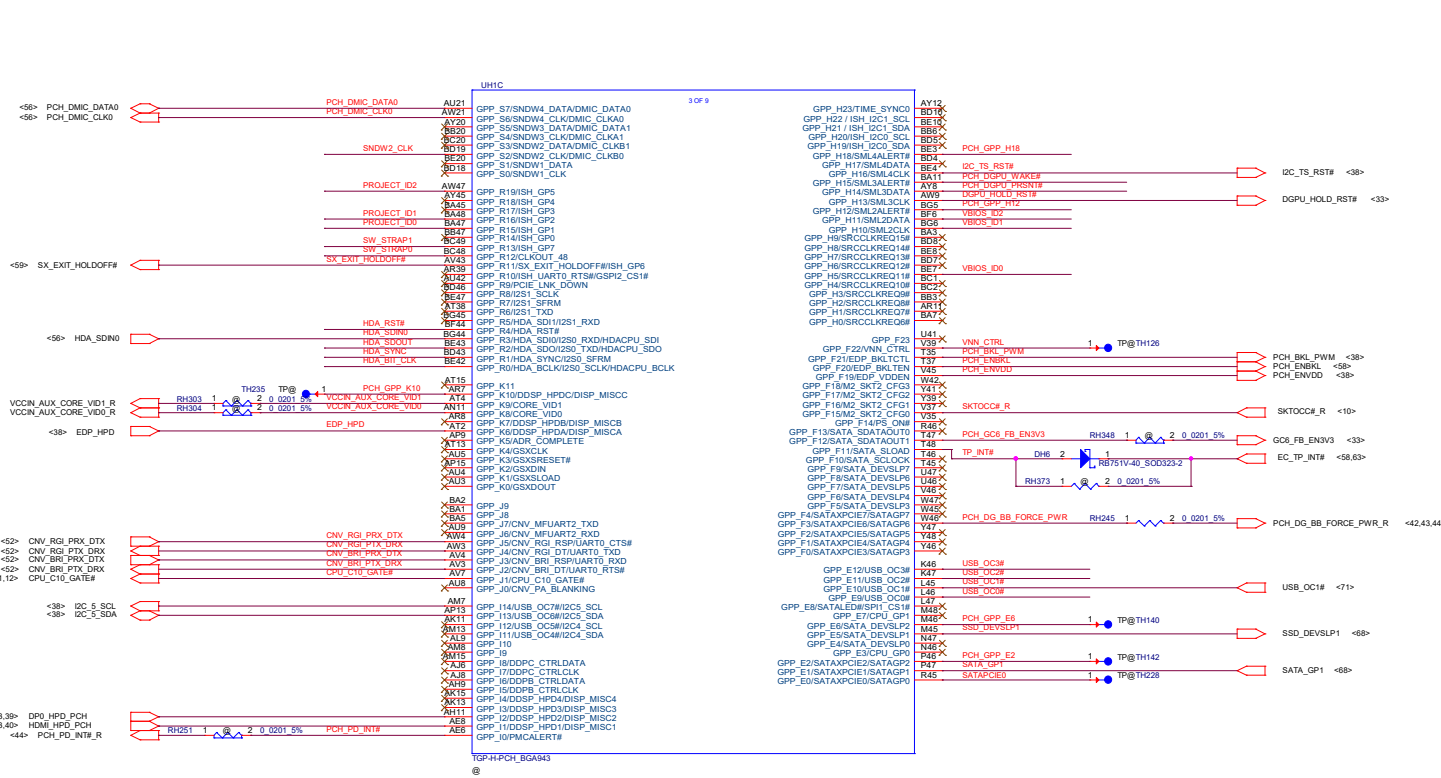
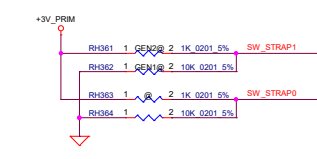
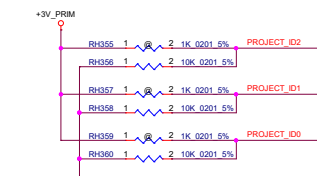
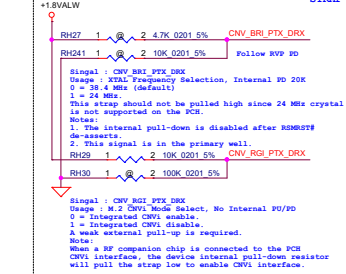
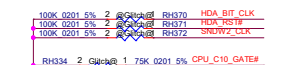
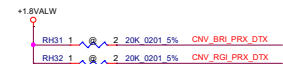
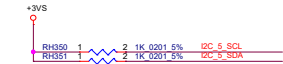
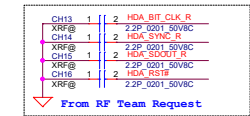
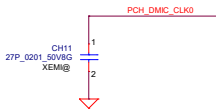
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	PCH(1/8)Clock/CNVi
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				Date	Thursday, March 18, 2021
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CPU

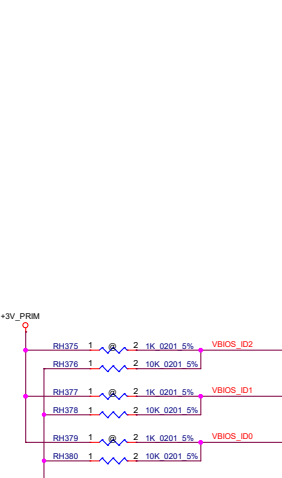


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2020/07/14	Deciphered Date	2021/12/31	Title	PCH(2/8)DMI
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					Document Number GH51G M/B LA-L181P
					Date: Thursday, March 18, 2021
					Sheet 15 of 121
					Rev 1A

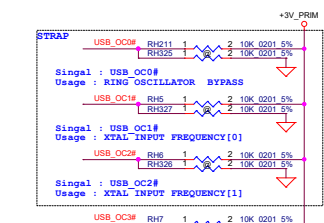
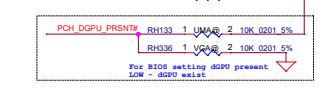
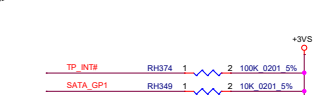
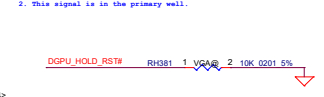
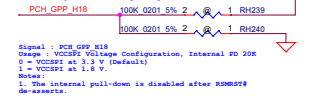
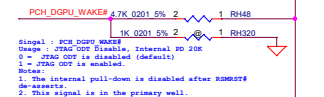
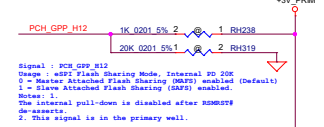


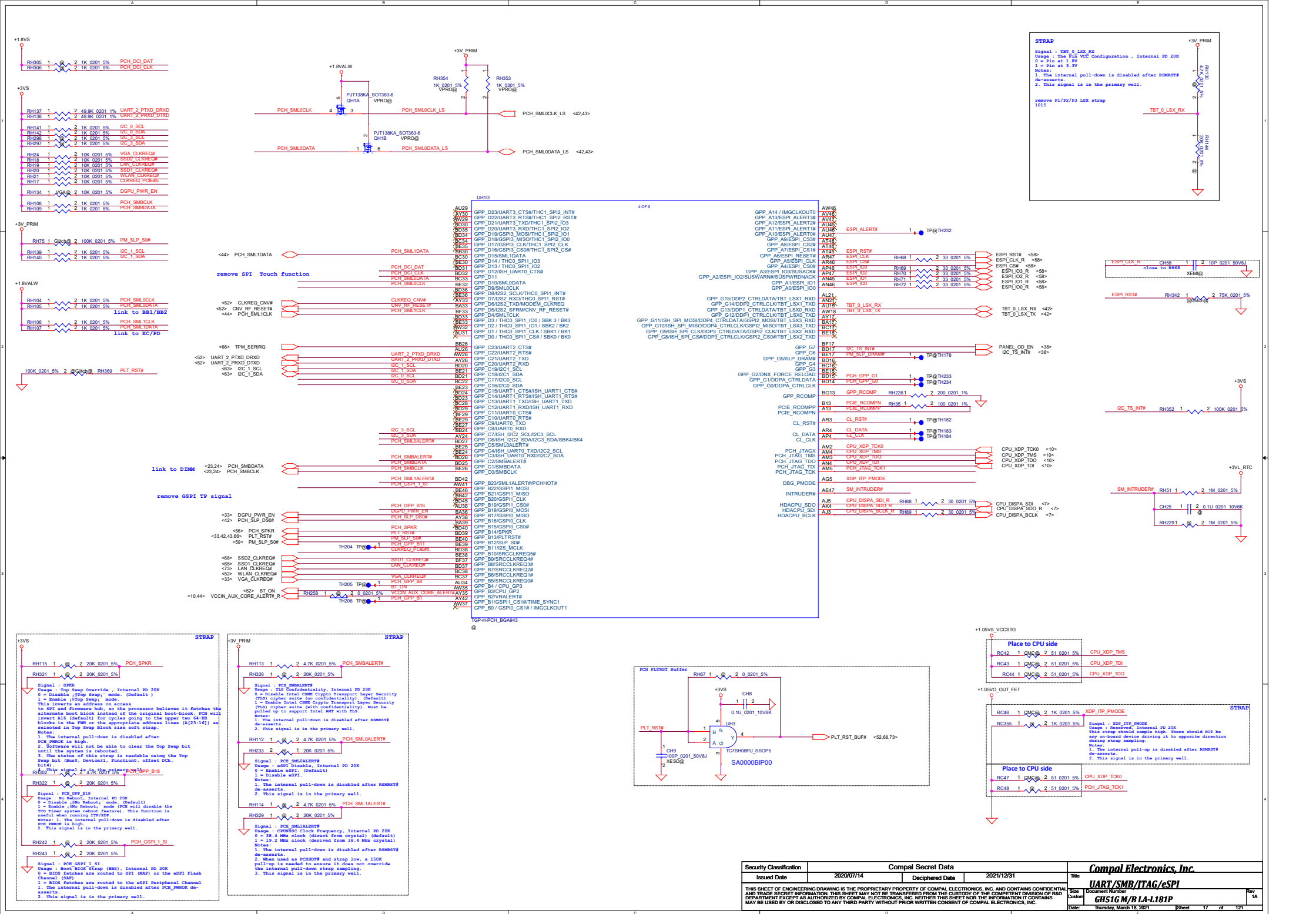
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Reserve	0	1	0
Reserve	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0
Reserve	1	1	1

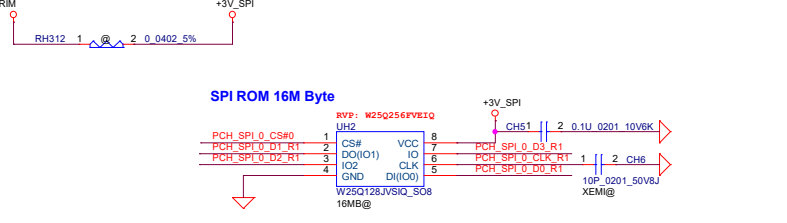
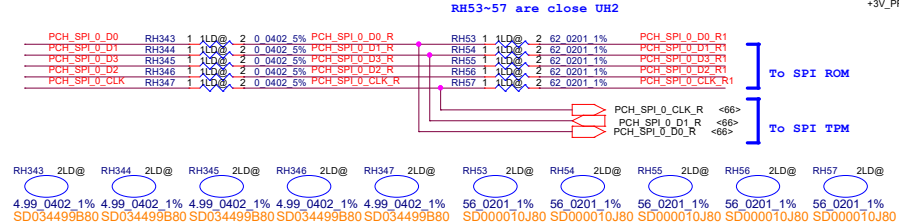
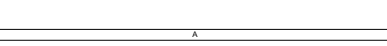
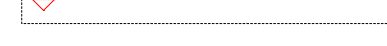
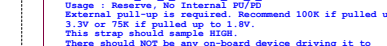
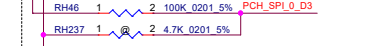
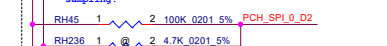
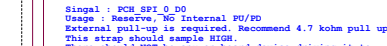
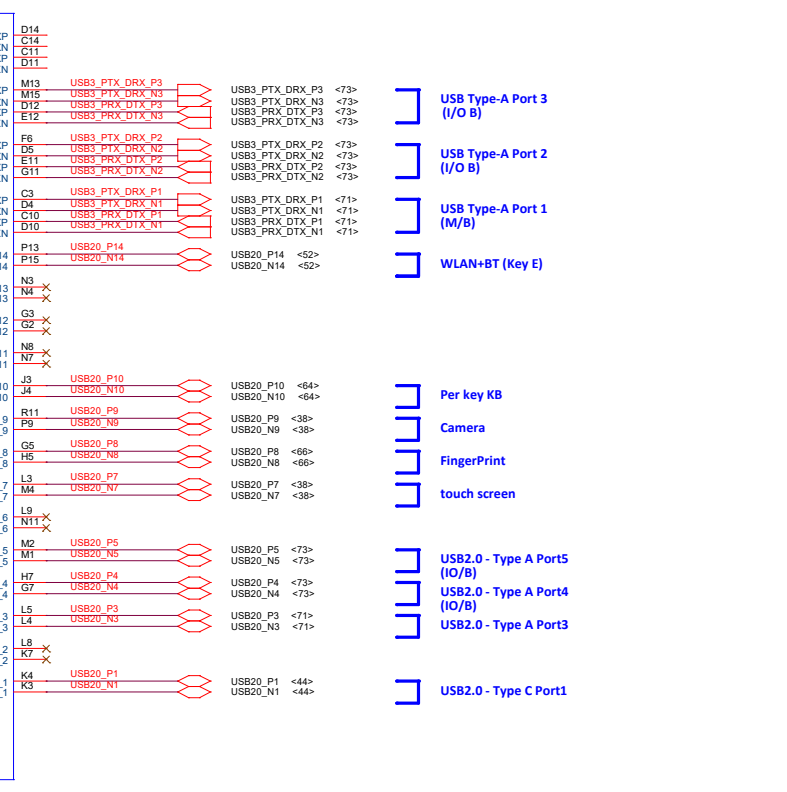
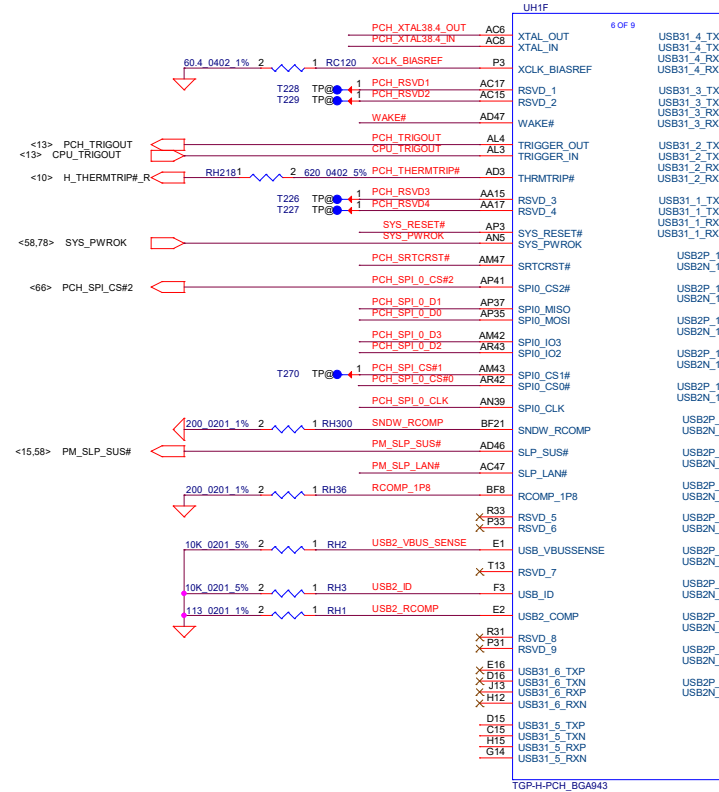
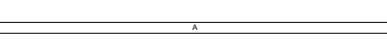
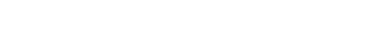
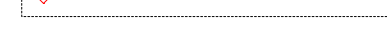
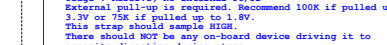
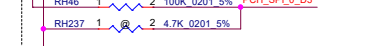
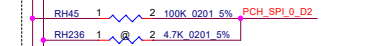
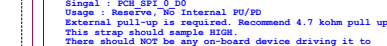
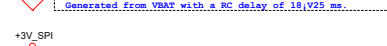
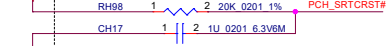
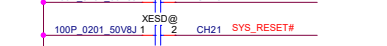
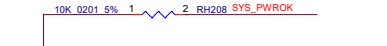
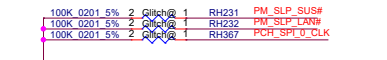
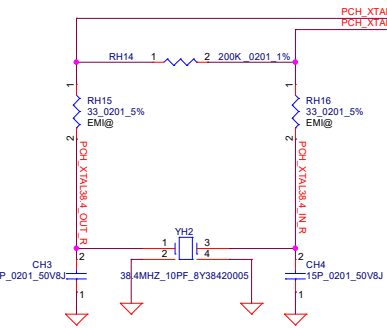
SW Strap_OVRM	SW_STRAP1 GPP_R13	SW_STRAP0 GPP_R12
*2021gaming 50 Gen1	0	0
2021gaming 60 Gen1	0	1
2021gaming 50 Gen2	1	0
2021gaming 60 Gen2	1	1



VBIOS ID	VBIOS_ID2 GPP_H11	VBIOS_ID1 GPP_H10	VBIOS_ID0 GPP_H5
*GH51G/GH71G	0	0	0
GH53G	0	0	1
GH73G	0	1	0
GH57G	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0
Reserve	1	1	1

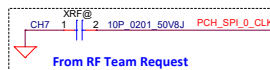
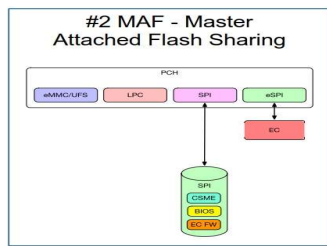




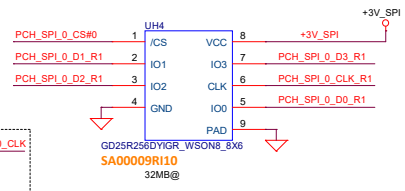


1. Length Matching between DATA and CLK should be Maximum of 500 mils.
2. Trace spacing between DATA and CLK should be 10 mils.
3. Trace spacing between CLK and other signals should be 15 mils.
4. SPI0_CLK & SPI0_CS# must be length matched to within 500 mils

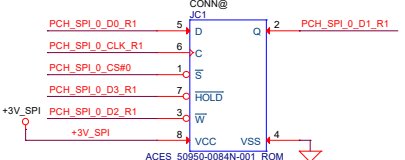
MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus



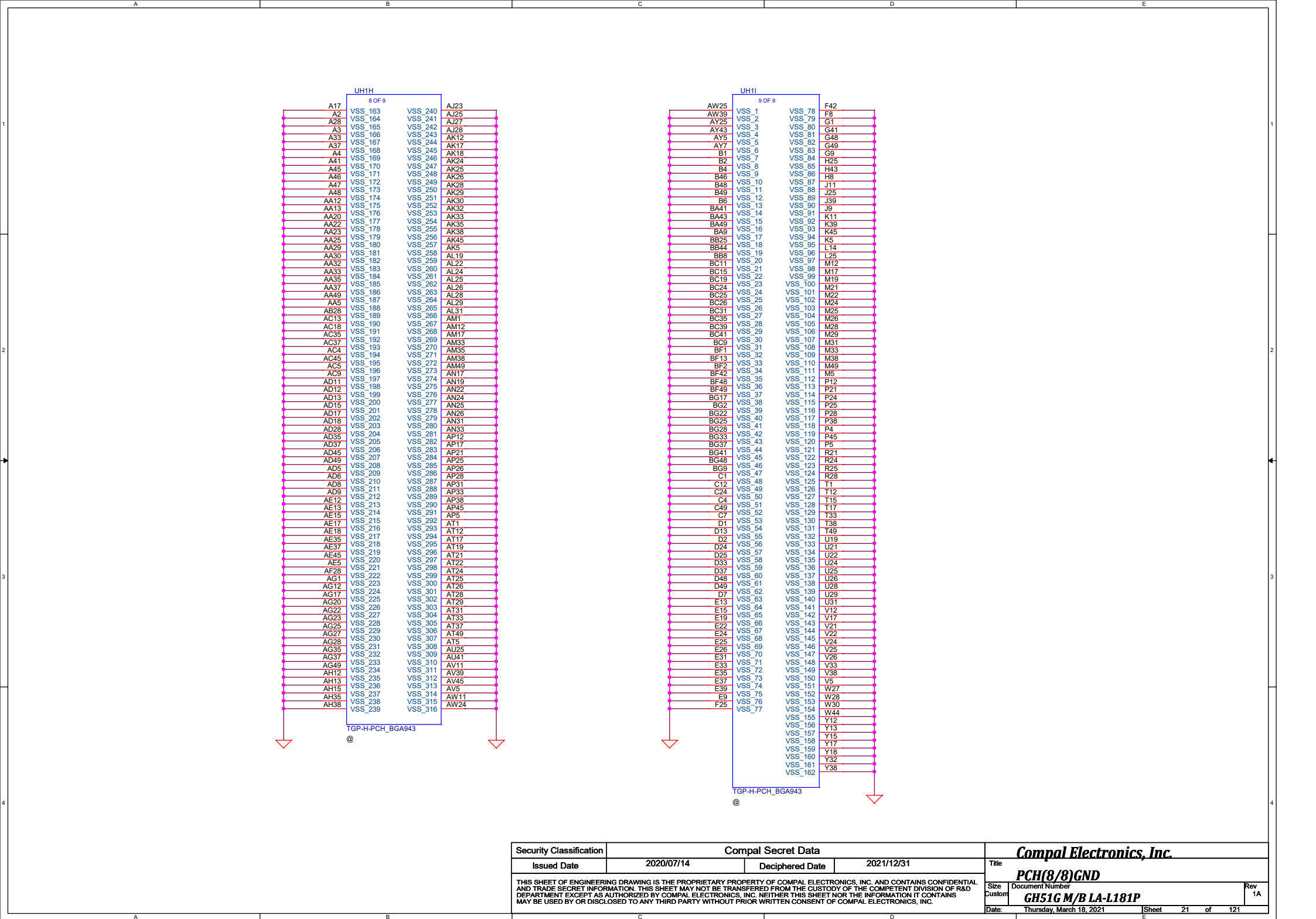
20200819 - 32M SPI ROM (WSON8)



ROM Socket



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Title		Compal Electronics, Inc.	
Document Number		PCH(6/8)USB2&3/SPI	
Size		GH51G M/B LA-L181P	
Date		Thursday, March 18, 2021	
Sheet		19 of 121	



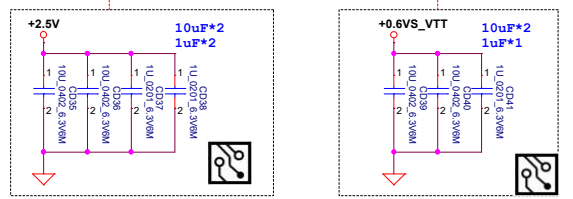
Reserve Page

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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	Reserve
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				Date	Thursday, March 18, 2021
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				Rev	1A

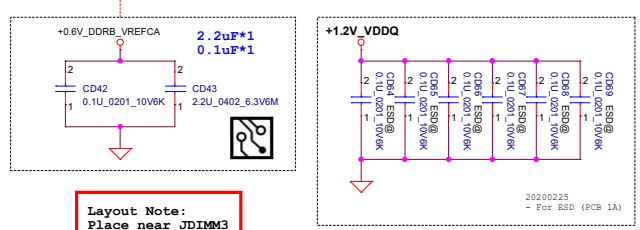
CHANNEL-B (Interleaved Memory)
> BOT : STD type (4mm)
> Non-ECC SO-DIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

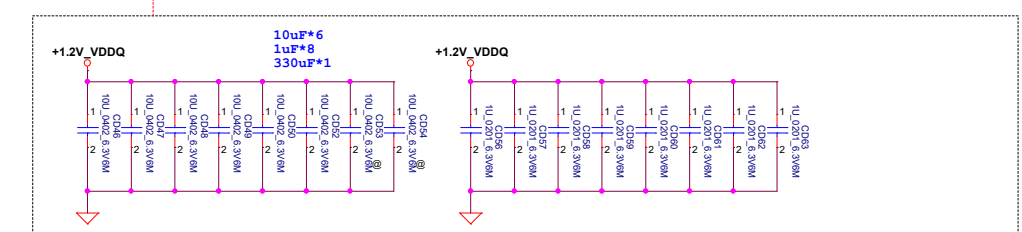
Layout Note:
Place near JDIMM3.257,259
Layout Note:
Place near JDIMM3.258



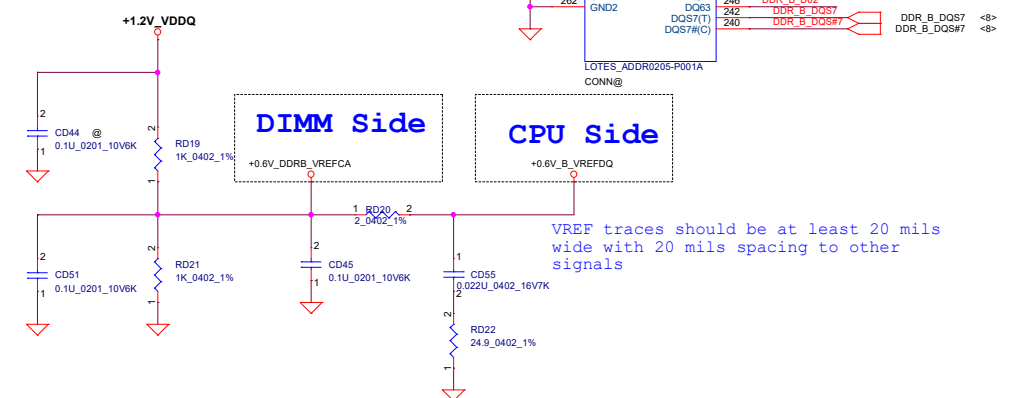
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3



Layout Note:
Place near JDIMM3



Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Reserve Page

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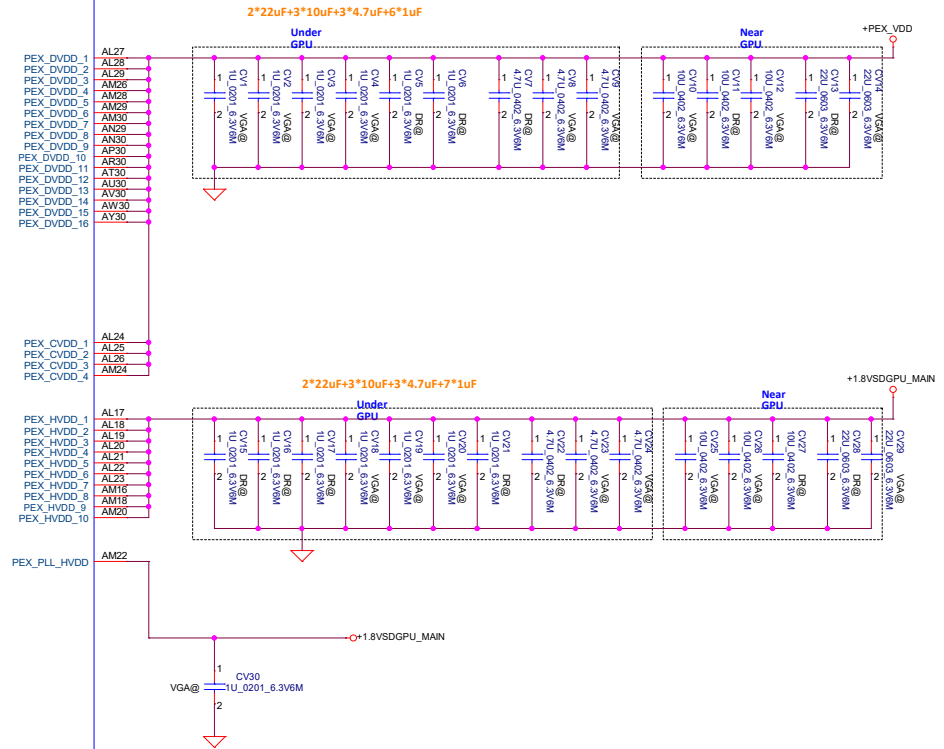
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	Reserve
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				Date	Thursday, March 18, 2021
				Sheet	26 of 121
				Rev	1A

UV1 N18PA@
S IC N18P-G61-A-A1 BGA 1358 GPU ABO !
SA0000DVM50

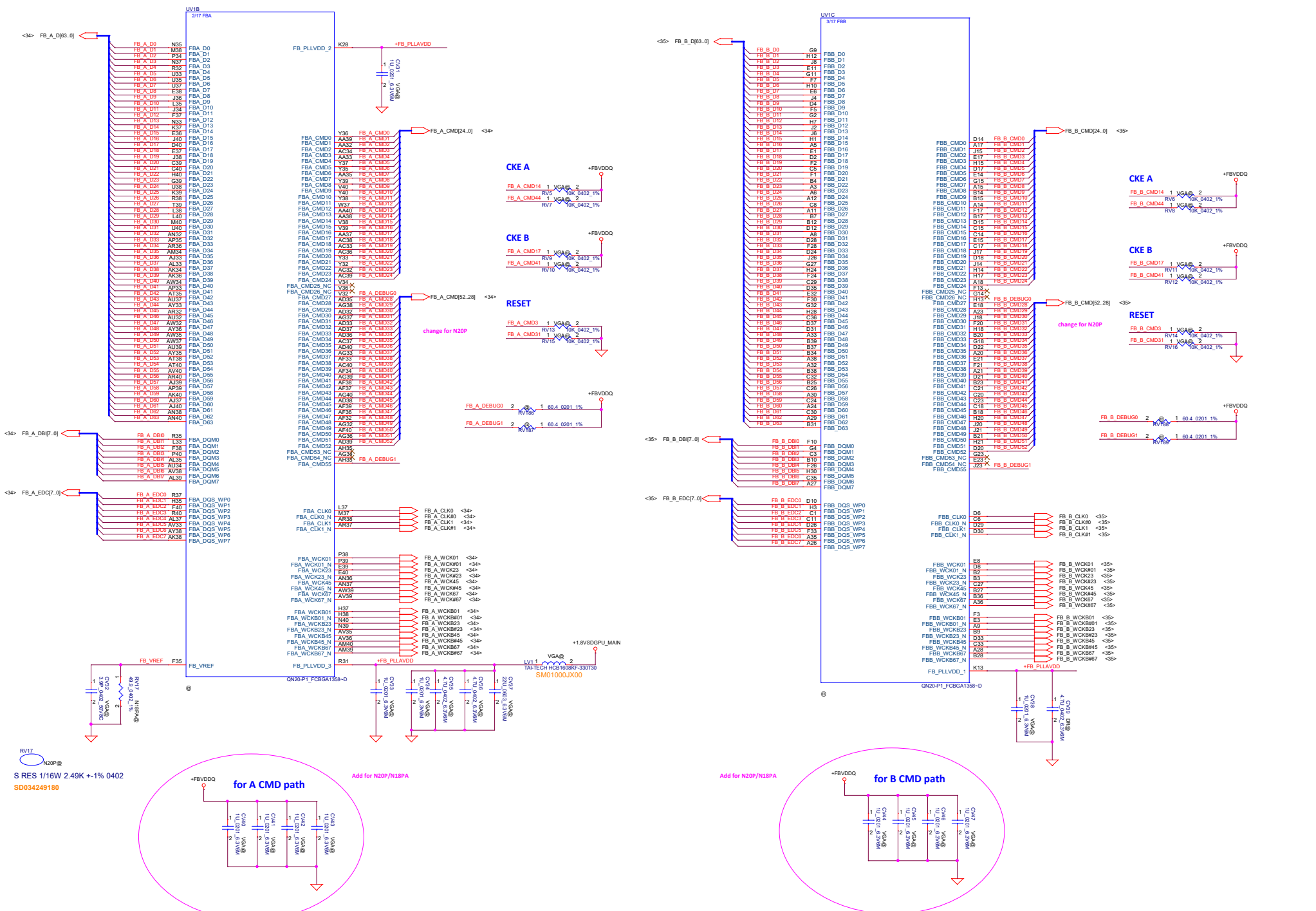
UV1 GN20P1@
S IC GN20-P1-A1 BGA 1358 GPU ABO !
SA0000DXQ40

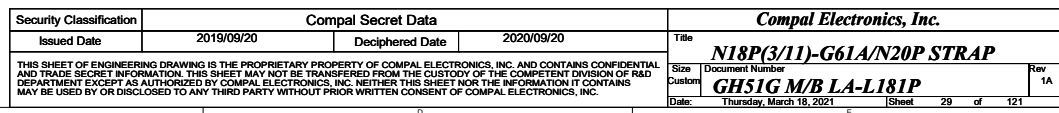
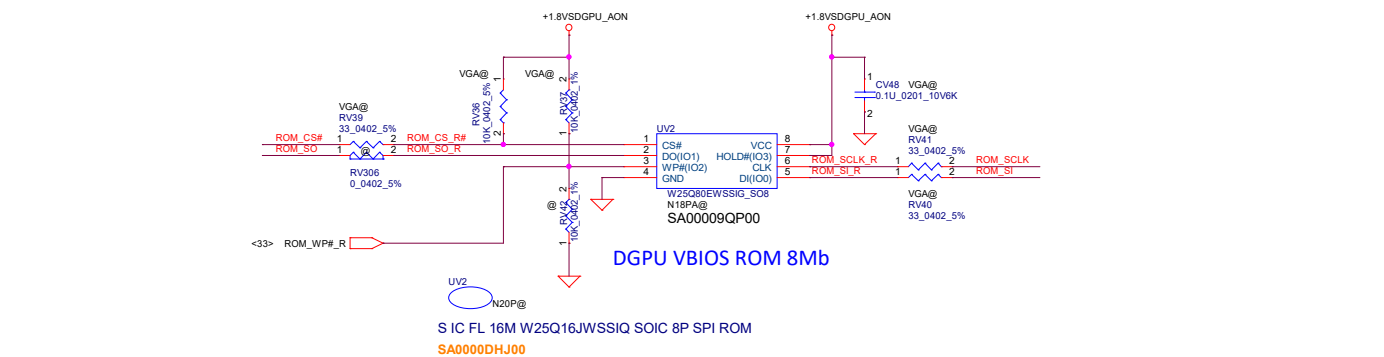
UV1 GN20P0@
S IC GN20-P0-A1 BGA 1358 GPU ABO !
SA0000EEC30

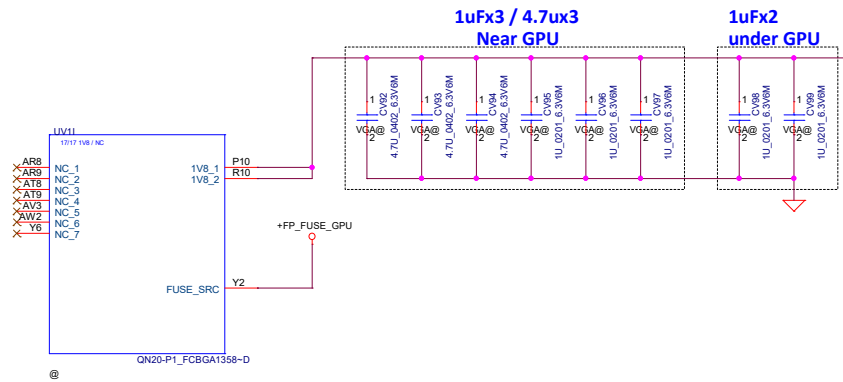
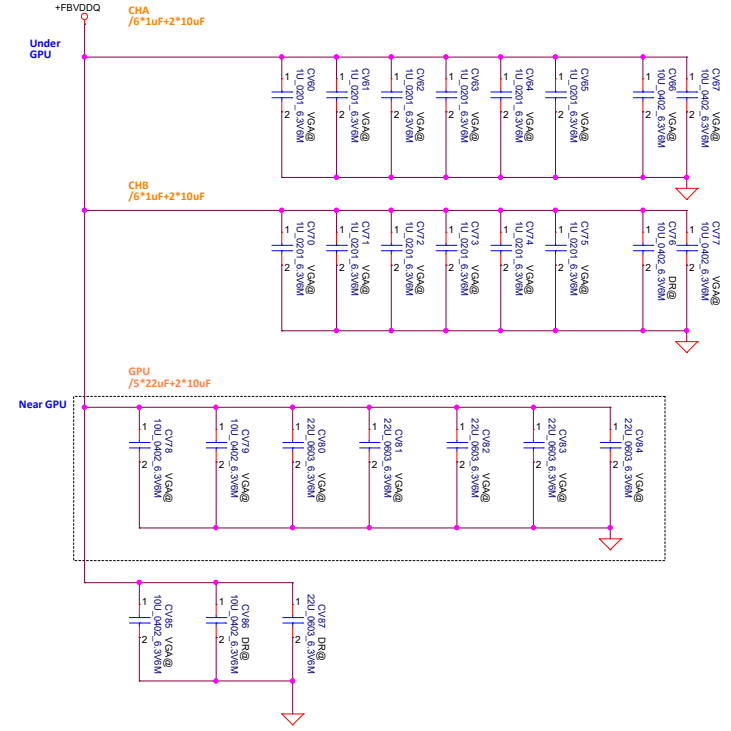
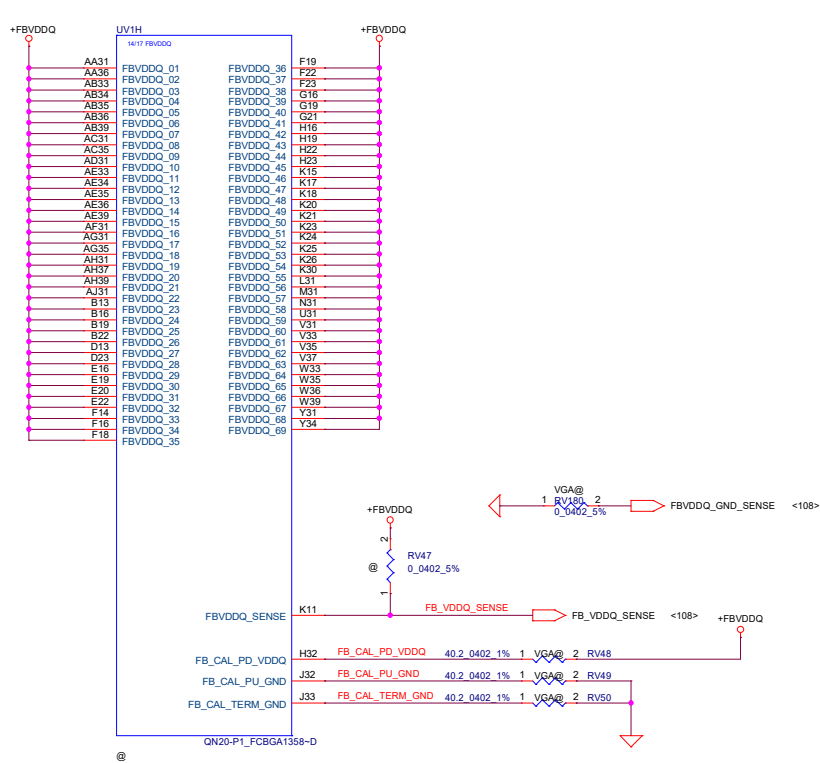
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SA0000EC30

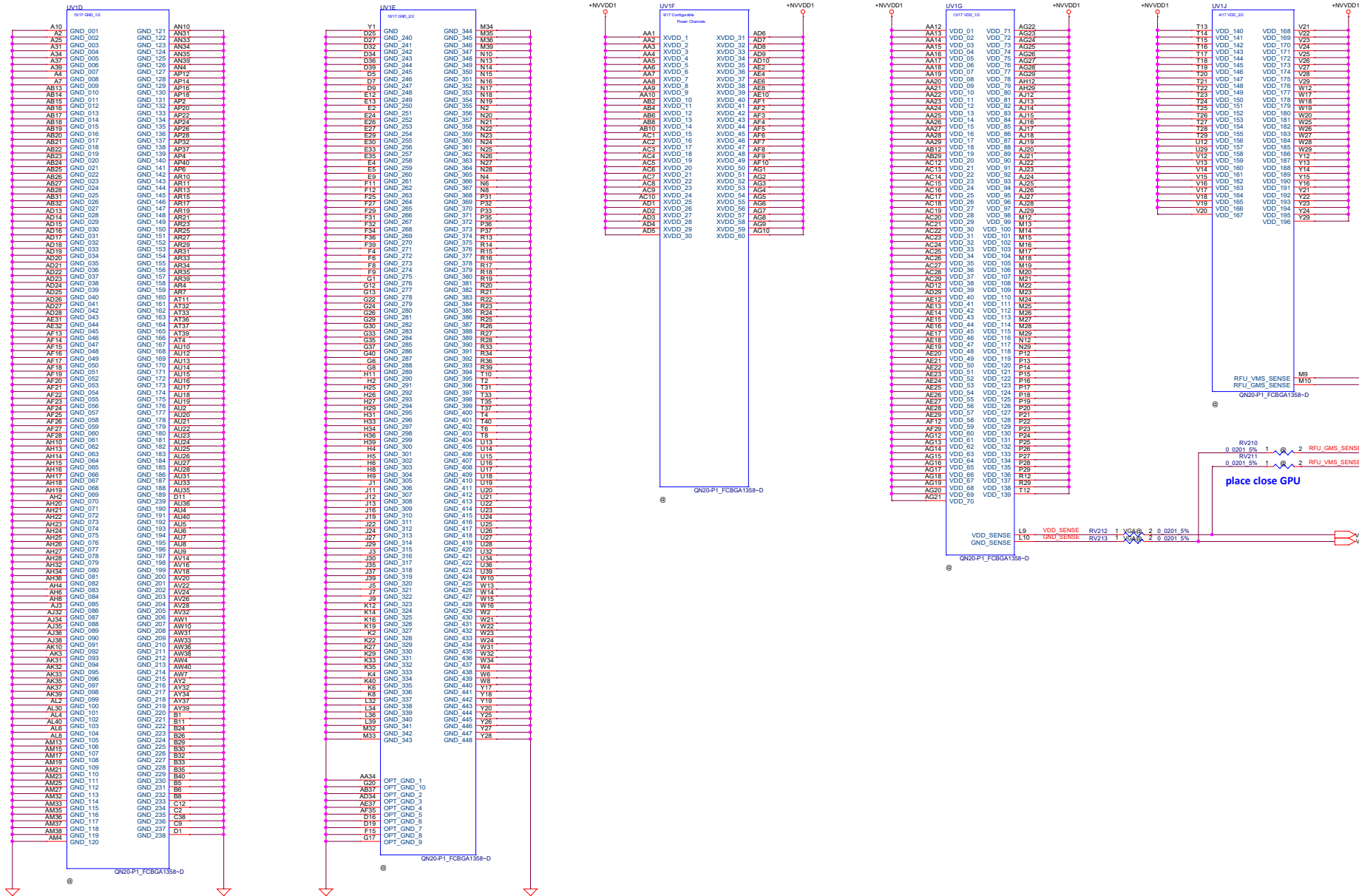
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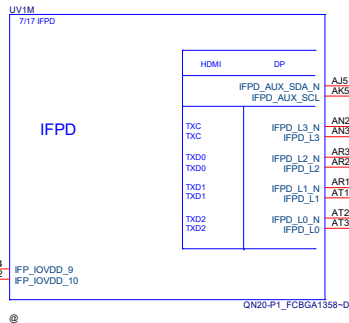
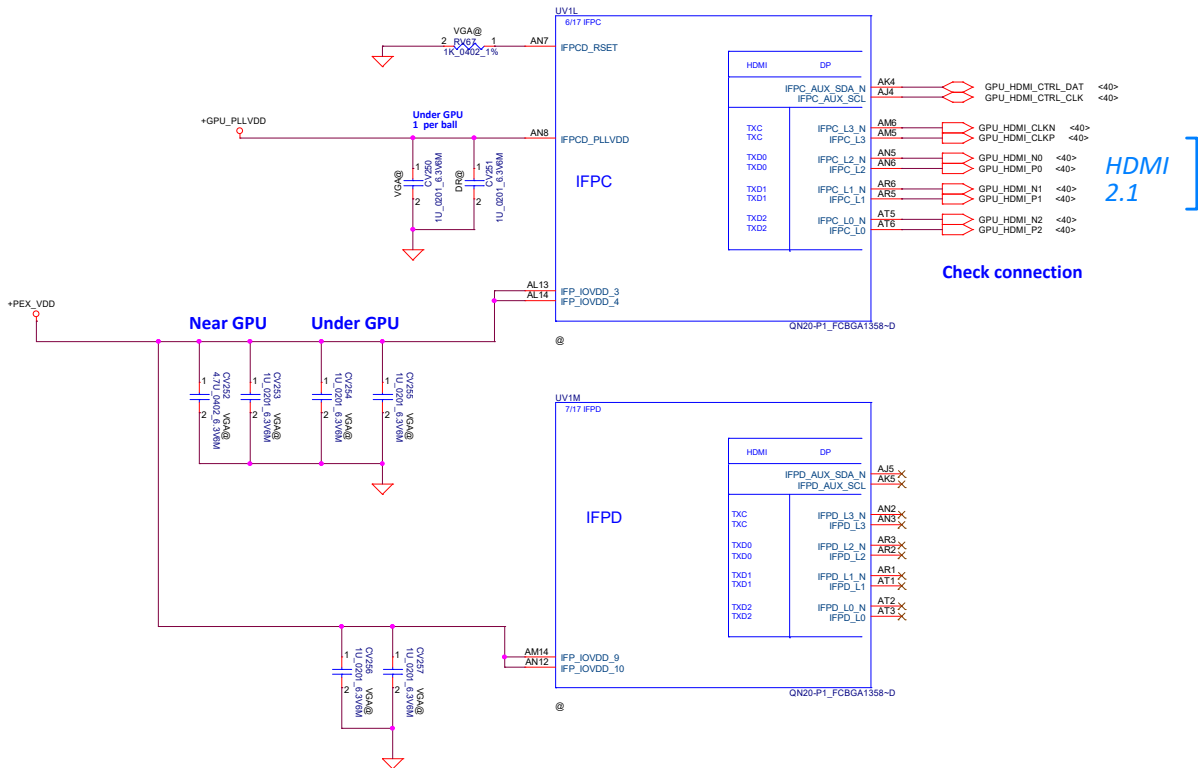
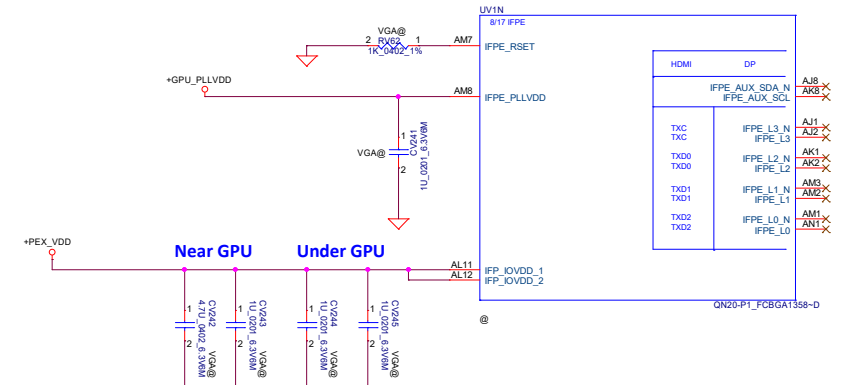
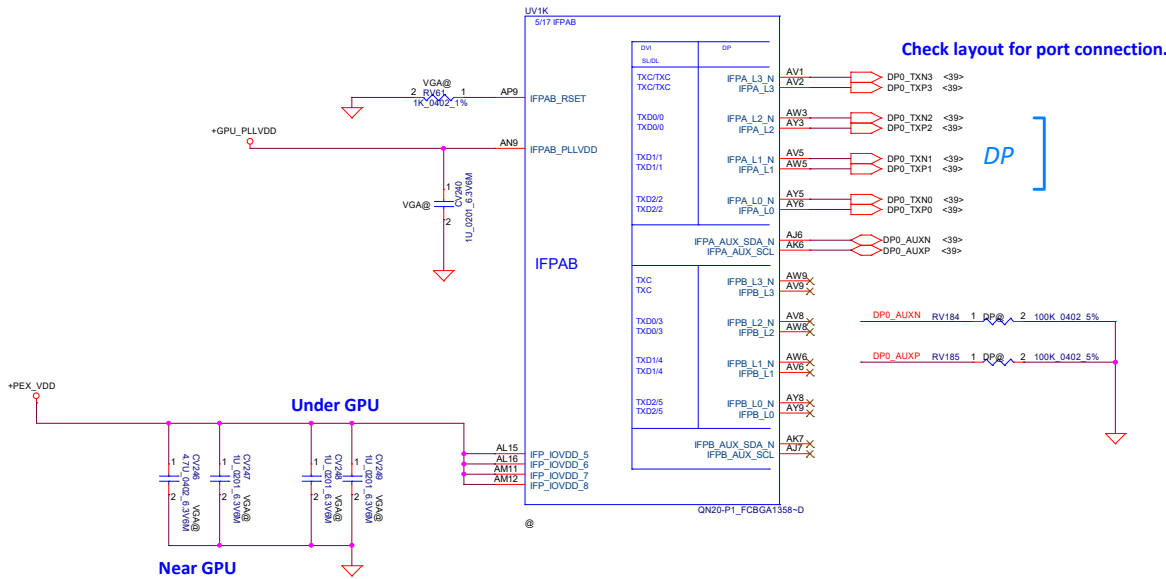
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18P(I/11)-G61A/N20P PEG		
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				Custom	GH51G M/B LA-L181P		
				Date:	Thursday, March 18, 2021	Sheet 27 of 121	

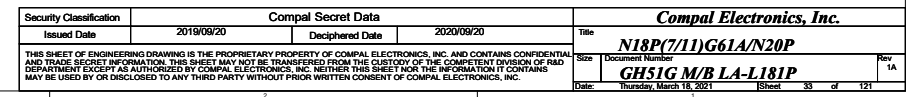
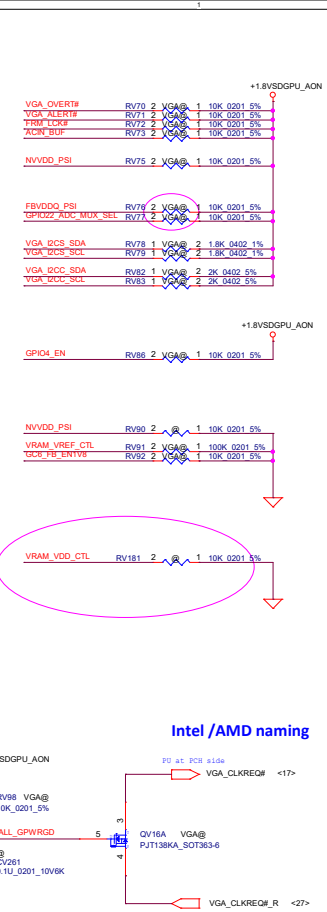




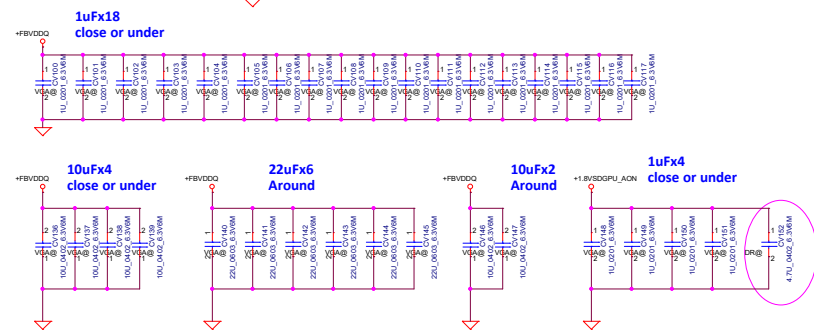
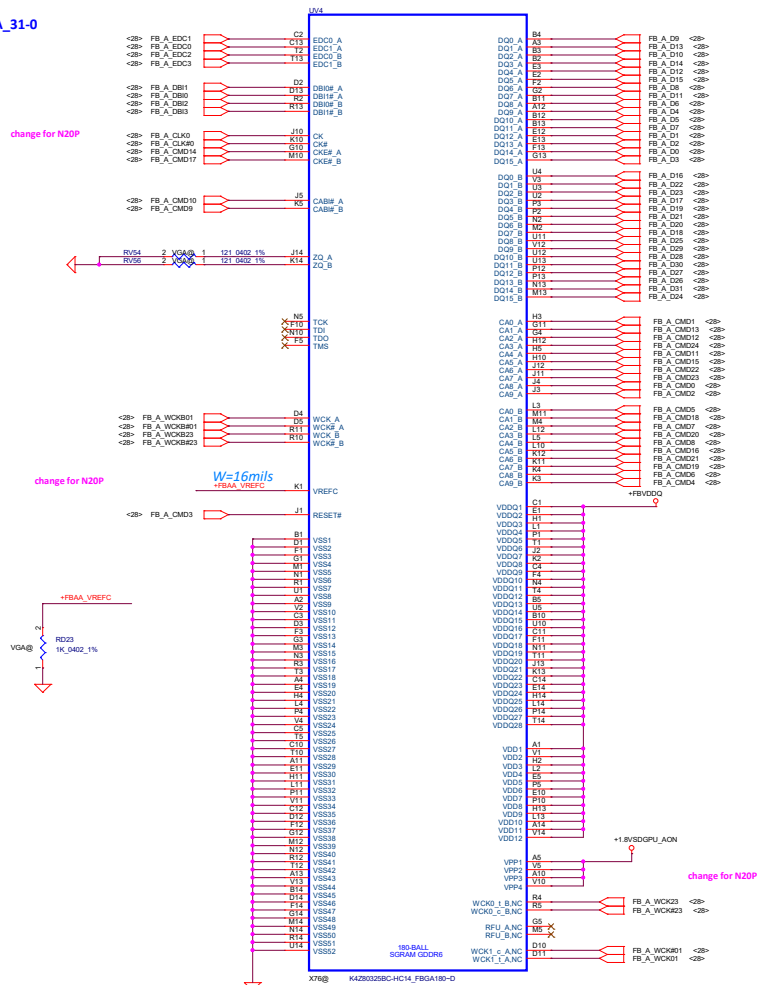




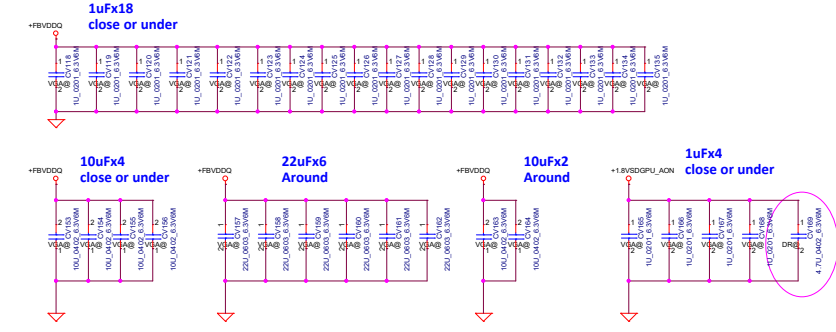
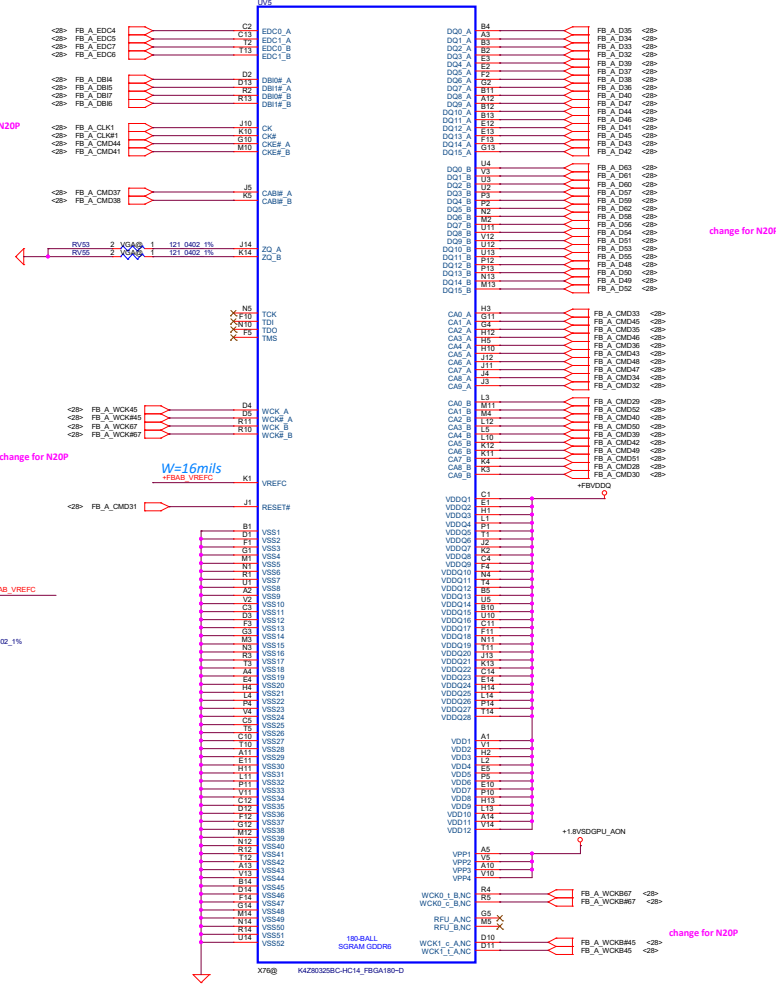


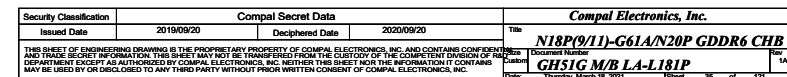
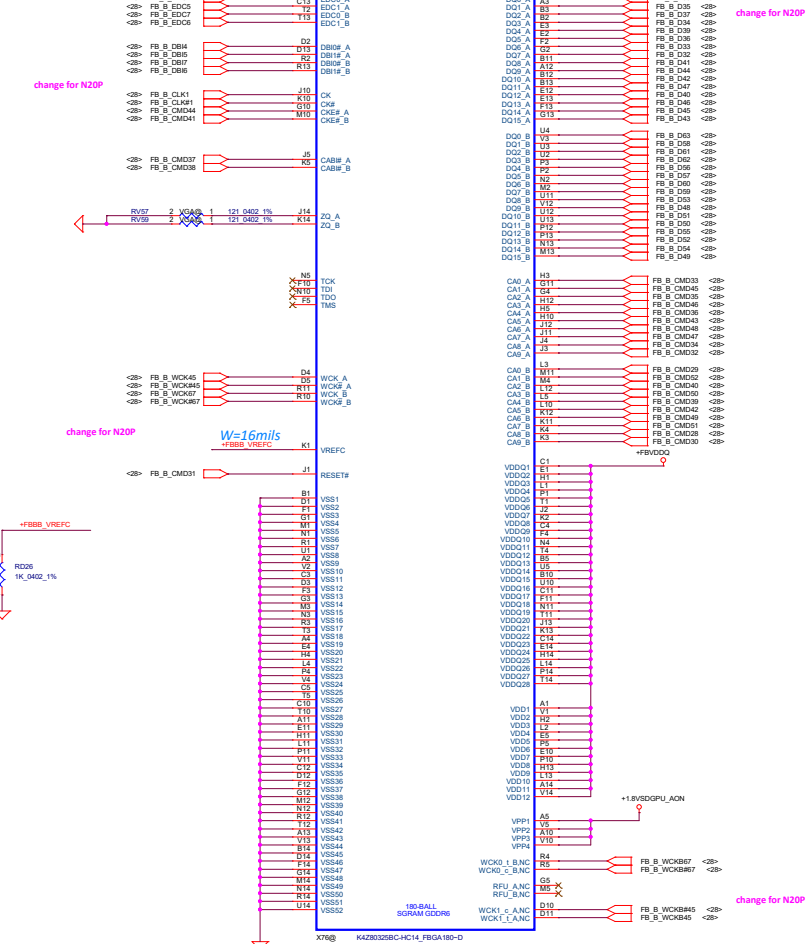
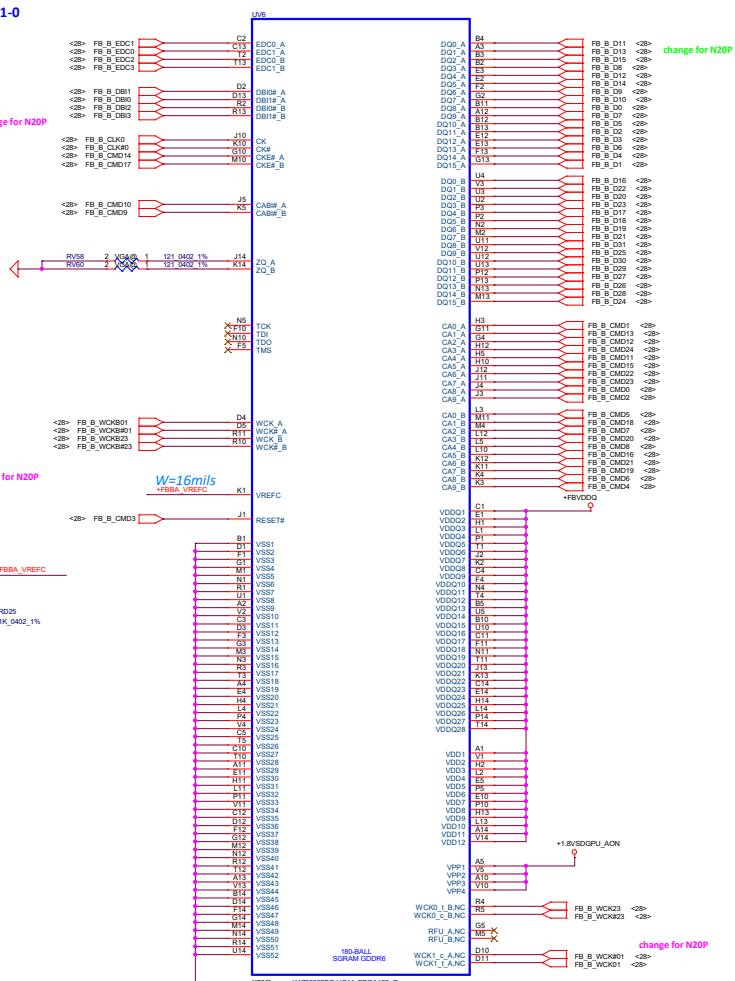


FBA_31-0



FBA_32-63



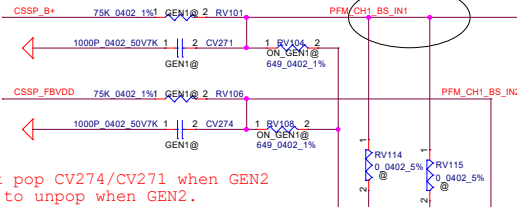


GEN2 gain control by VBIOS

RV101 GEN2@
0_0402_5%
SD028000080

RV106 GEN2@
0_0402_5%
SD028000080

NV Suggest



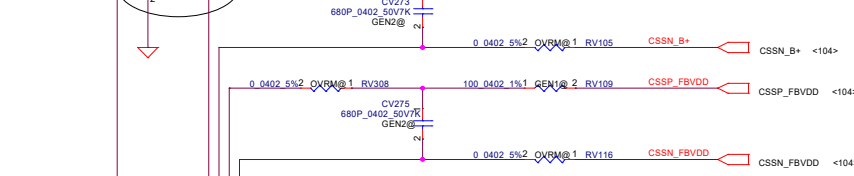
For OVRM Keep ON

GEN2 gain control by VBIOS

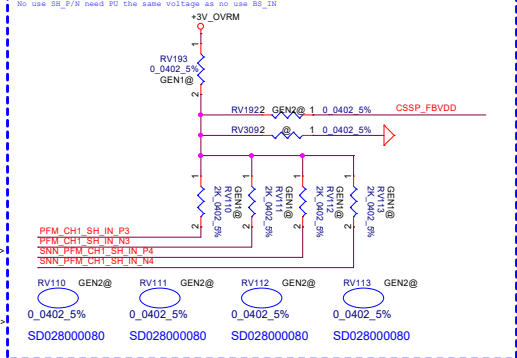
RV103 GEN2@
0_0402_5%
SD028000080

RV109 GEN2@
0_0402_5%
SD028000080

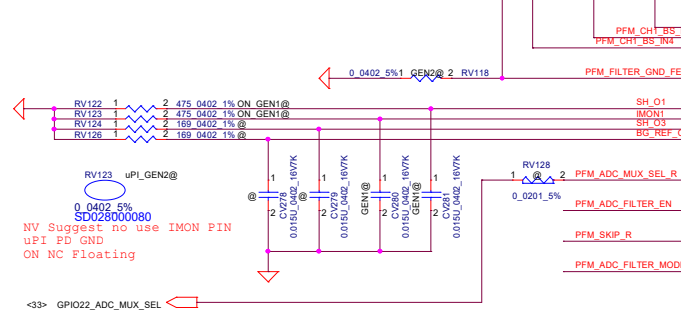
NV Suggest



GEN2 NV suggest BS_1N3,4 need also connect with BS_1N2(CSSP_FBVDD)
No use SH_P/N need PD the same voltage as no use BS_1N



UPI-Semi suggest pop CV274/CV271 when GEN2
Keep NV suggest to unpop when GEN2.



SA0000CQX00

NC P45482XMTWG_QFN32_4X4

ON_GEN1@

BS_IN1

BS_IN2

BS_IN3

BS_IN4

SH_IN_P1

SH_IN_P2

SH_IN_P3

SH_IN_P4

SH_IN_P5

SH_IN_P6

SH_IN_P7

SH_IN_P8

SH_IN_P9

SH_IN_P10

SH_IN_P11

SH_IN_P12

SH_IN_P13

SH_IN_P14

SH_IN_P15

SH_IN_P16

SH_IN_P17

SH_IN_P18

SH_IN_P19

SH_IN_P20

SH_IN_P21

SH_IN_P22

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SH_IN_P25

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SH_IN_P28

SH_IN_P29

SH_IN_P30

SH_IN_P31

SH_IN_P32

SH_IN_P33

SH_IN_P34

SH_IN_P35

SH_IN_P36

SH_IN_P37

SH_IN_P38

SH_IN_P39

SH_IN_P40

SH_IN_P41

SH_IN_P42

SH_IN_P43

SH_IN_P44

SH_IN_P45

SH_IN_P46

SH_IN_P47

SH_IN_P48

SH_IN_P49

SH_IN_P50

SH_IN_P51

SH_IN_P52

SH_IN_P53

SH_IN_P54

SH_IN_P55

SH_IN_P56

SH_IN_P57

SH_IN_P58

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SH_IN_P66

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SH_IN_P70

SH_IN_P71

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SH_IN_P111

SH_IN_P112

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SH_IN_P115

SH_IN_P116

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SH_IN_P166

SH_IN_P167

SH_IN_P168

SH_IN_P169

SH_IN_P170

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SH_IN_P173

SH_IN_P174

SH_IN_P175

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SH_IN_P177

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SH_IN_P216

SH_IN_P217

SH_IN_P218

SH_IN_P219

SH_IN_P220

SH_IN_P221

SH_IN_P222

SH_IN_P223

SH_IN_P224

SH_IN_P225

SH_IN_P226

SH_IN_P227

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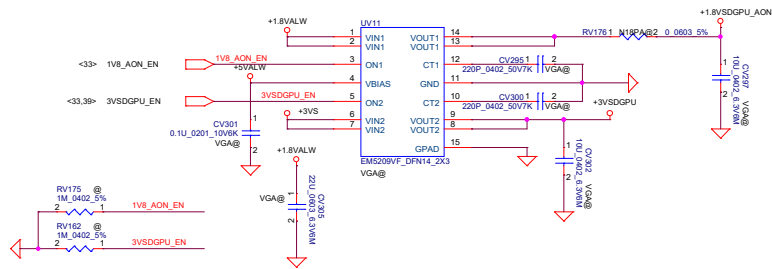
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SH_IN_P249

SH_IN_P250

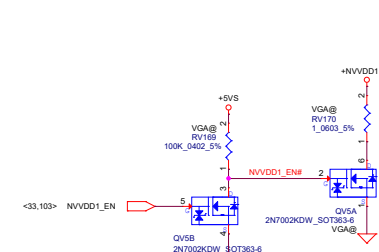
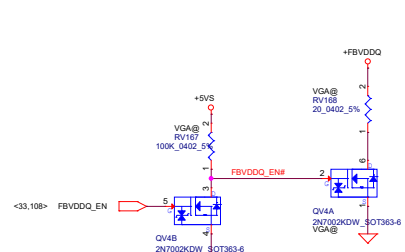
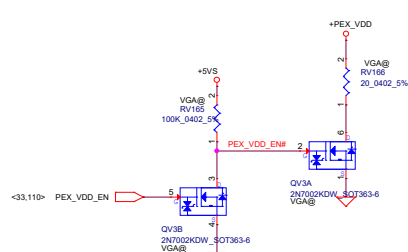
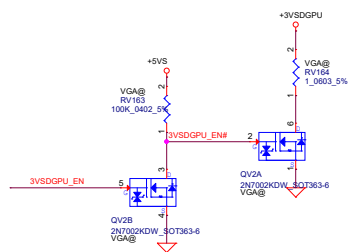
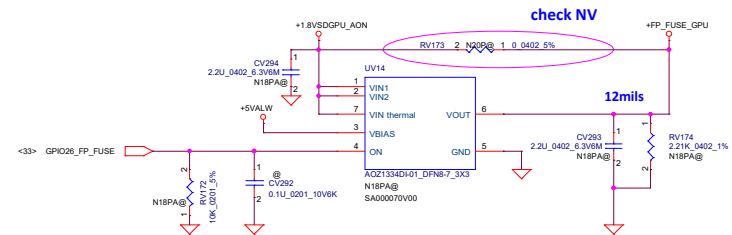
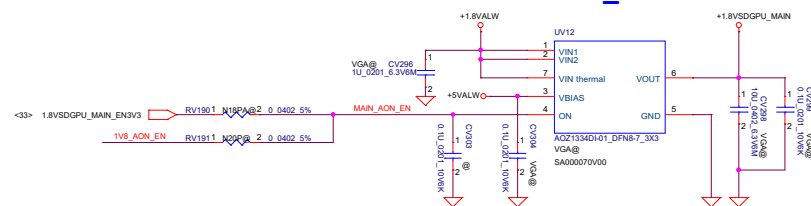
+1.8V_AON/+3VSDGPU



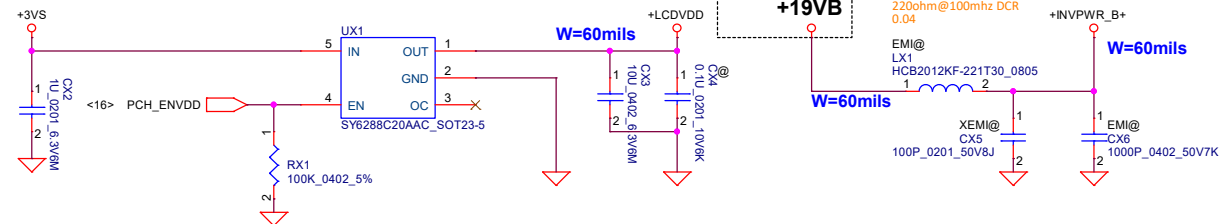
For VGA bracket.



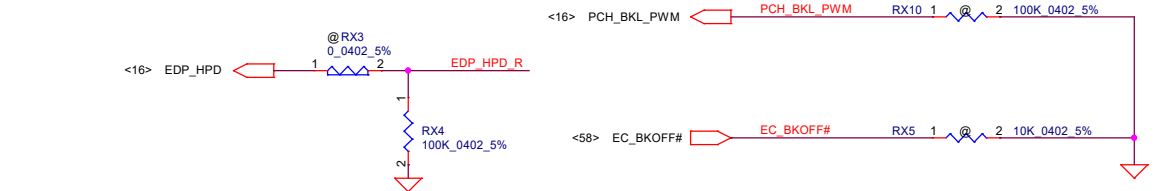
+1.8V_MAIN



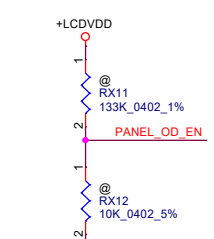
LCD POWER CIRCUIT



LCD enable signal

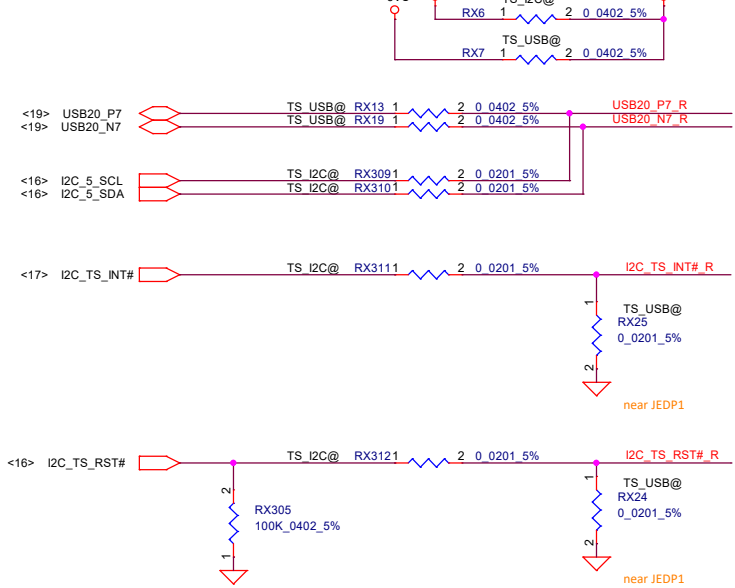


Panel OD

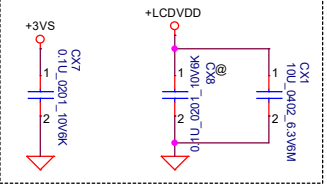


20190506
- RX11 change to unpop
- BIOS needs to detect panel
to select R or L .

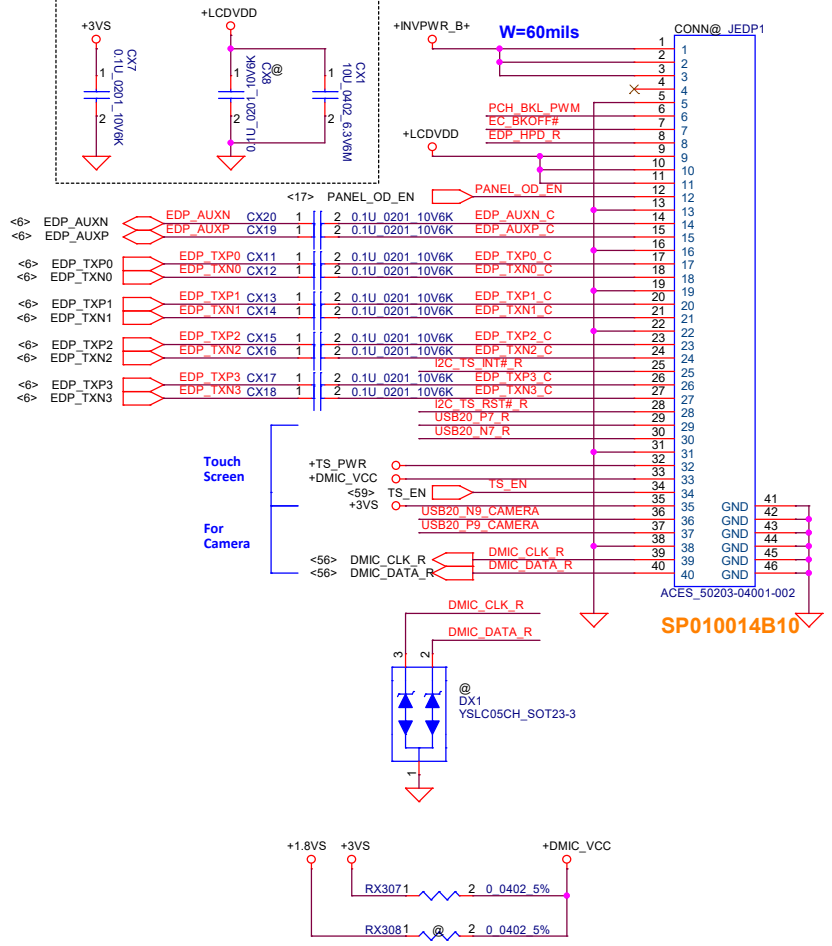
USB/I2C Touch Screen Co-Lay



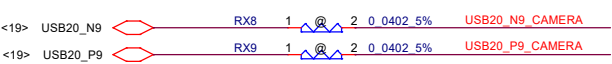
Place closed to JEDP1



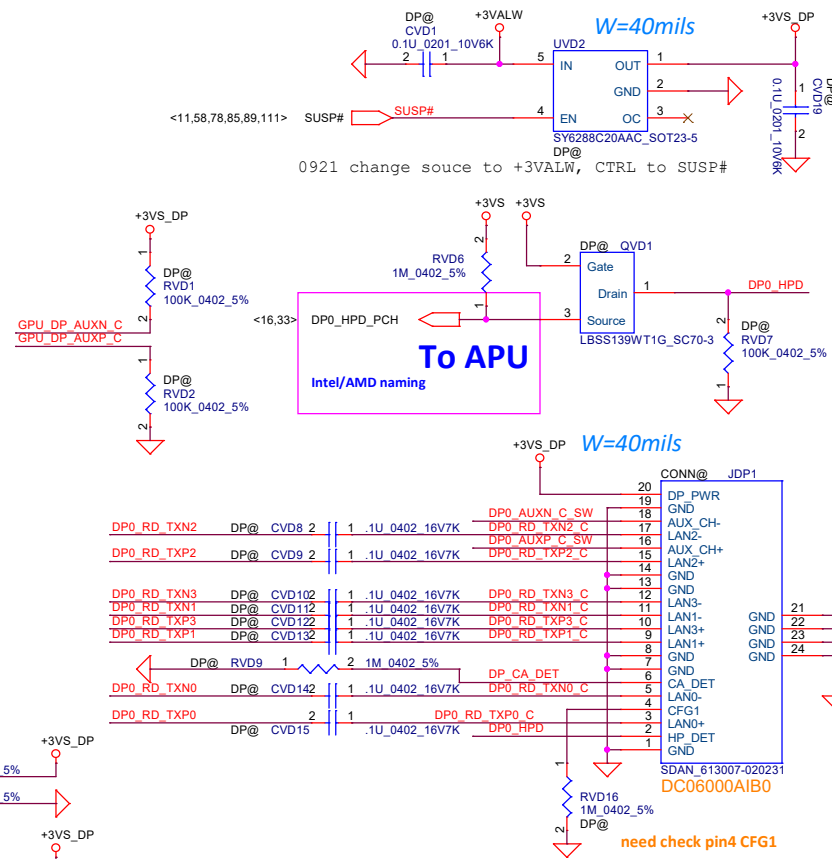
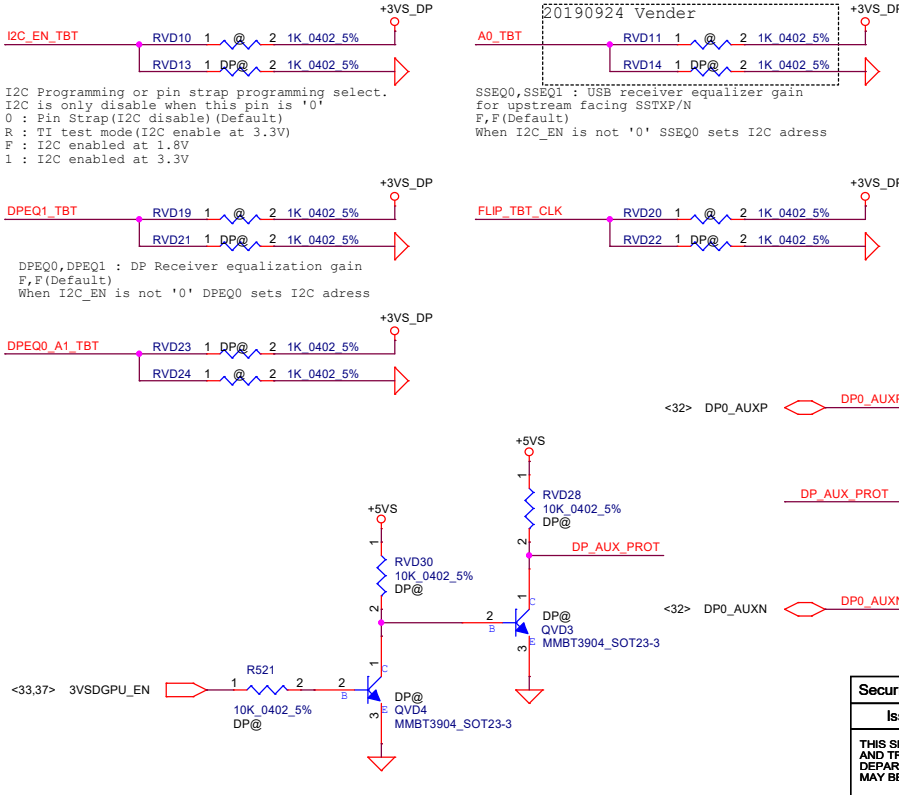
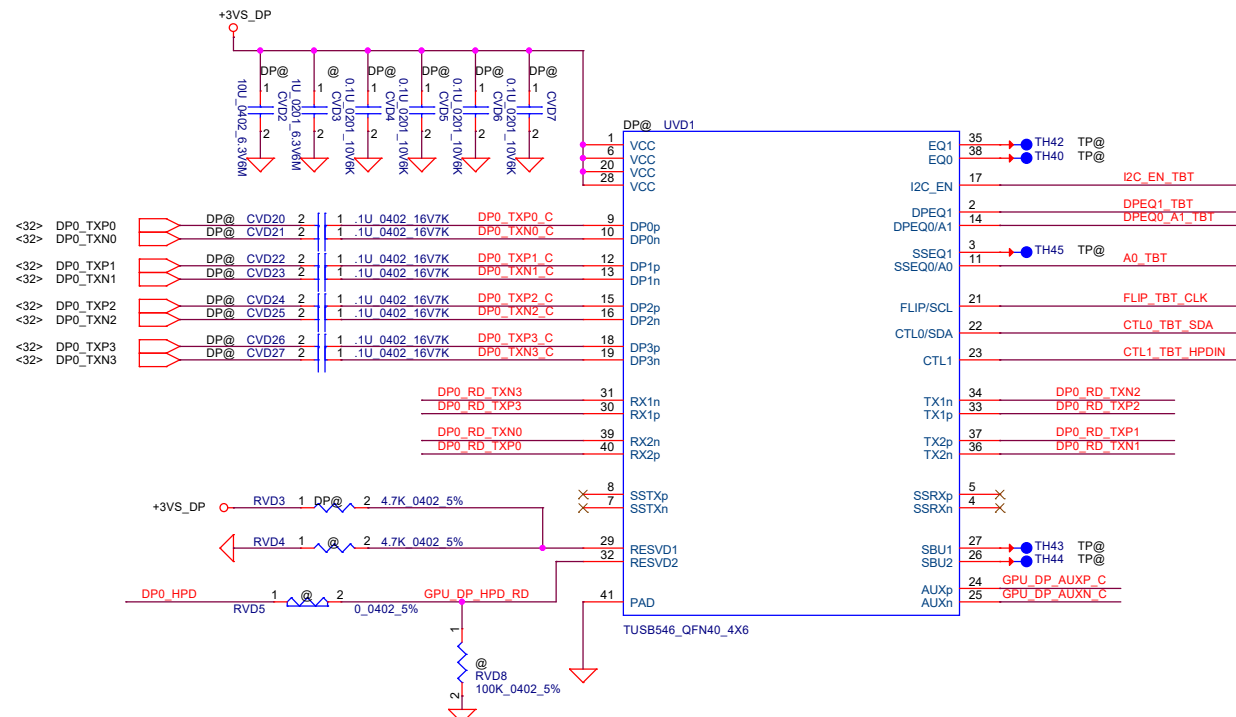
LED PANEL Conn.



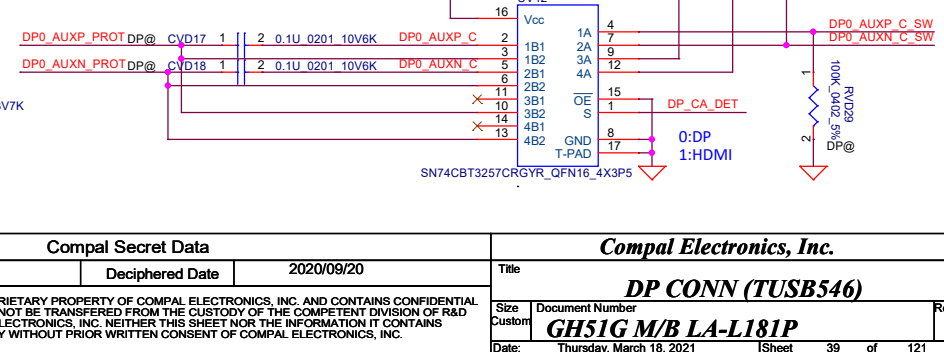
CAMERA

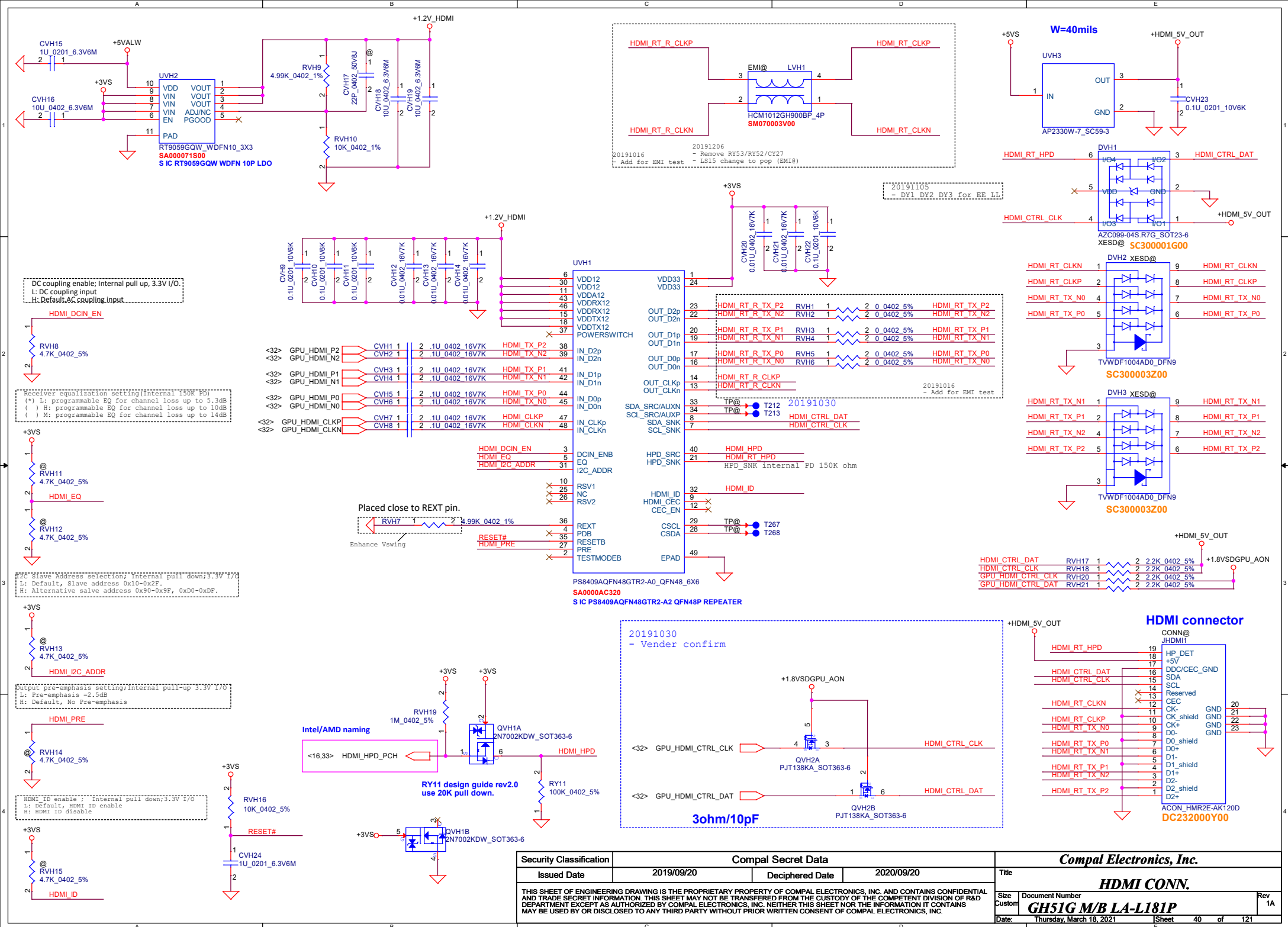


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								Size	Document Number	Rev
								Custom	GHS1G M/B LA-L181P	1A
								Date:	Thursday, March 18, 2021	Sheet



OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

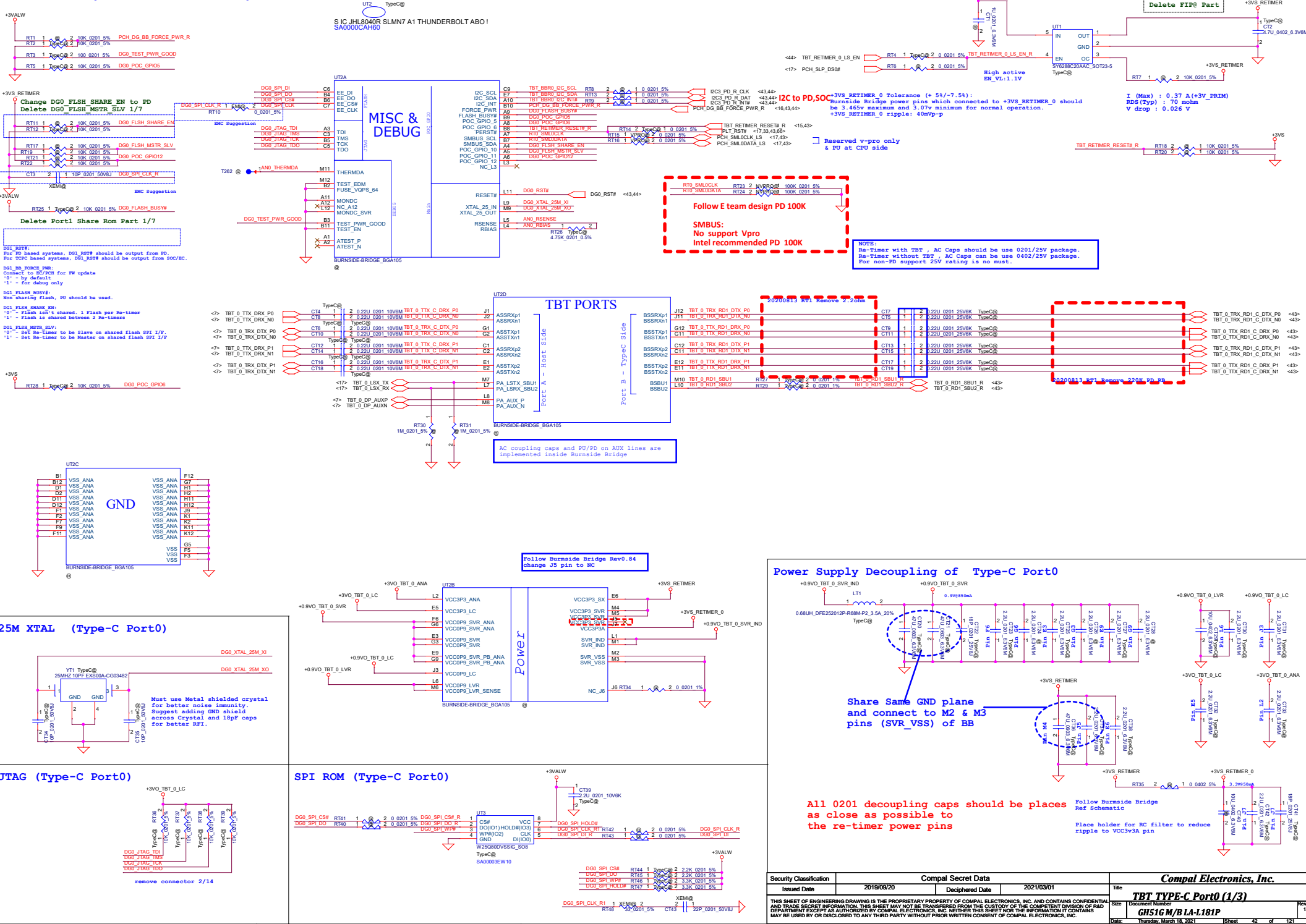




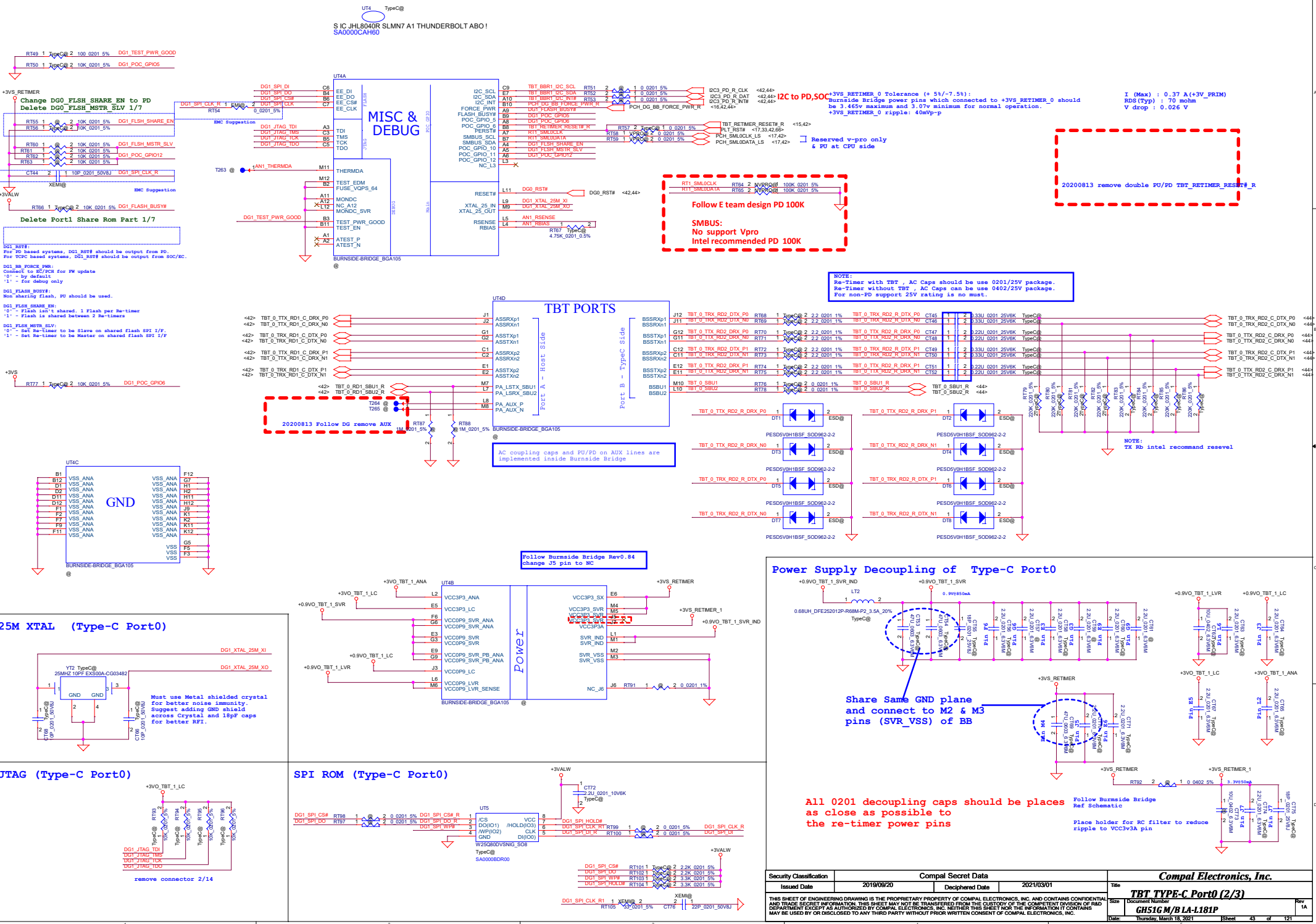
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				Sheet	41 of 121
				Rev	1A

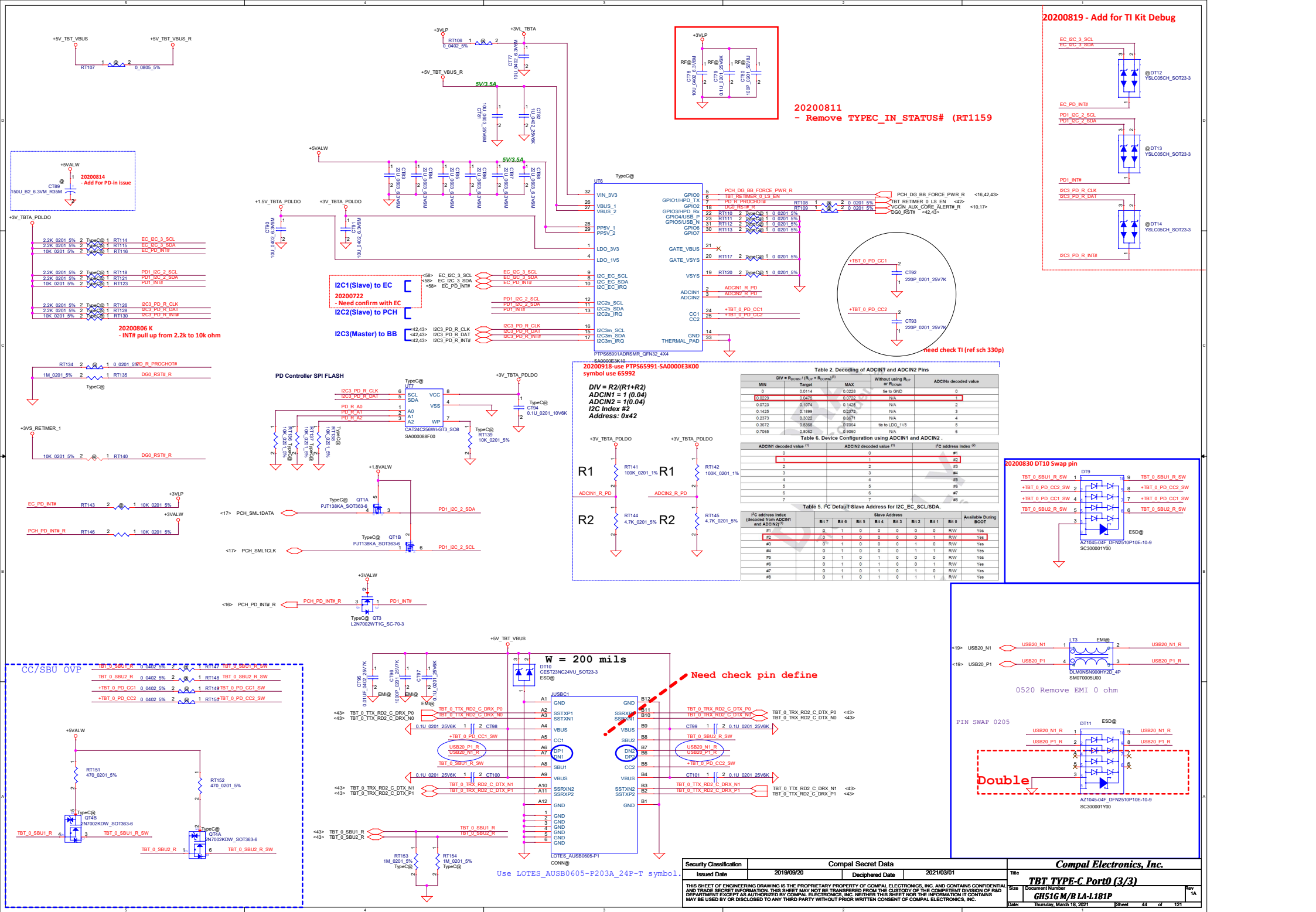
TBT Conn. (Port 0/ Re-Timer1)



TBT Conn. (Port 0/ Re-Timer2)



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2019/09/20	Deciphered Date	2021/03/01	Title	TBT TYPE-C Port0 (2/3)	
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20200819 - Add for TI Kit Debug

20200811
- Remove TYPEC_IN_STATUS# (RT1159)

Need check TI (ref sch 330p)

20200830 DT10 Swap pin

Need check pin define

Double

Security Classification		Compal Secret Data		2021/03/01		Title		Compal Electronics, Inc.	
Issued Date		Deciphered Date		2021/03/01		TBT Type-C Port0 (3/3)		Rev 1A	
Size		Document Number		GH51G M/B LA-181P		Date		Thursday, March 18, 2021	
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				Date	Thursday, March 18, 2021
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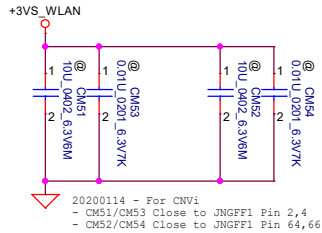
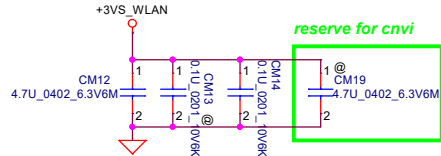
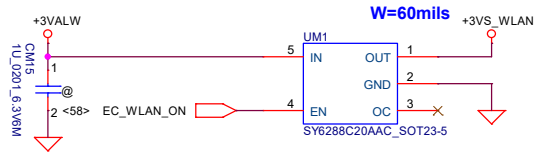
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20190918
LAN more to IO/B

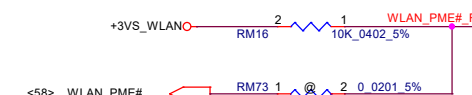
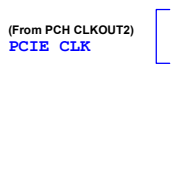
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2019/09/20		2020/09/20		LAN Killer-E2600	
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Wireless LAN

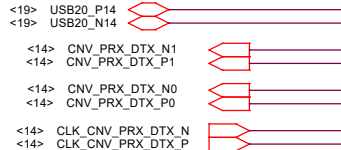


NGFF WL+BT (KEY E)

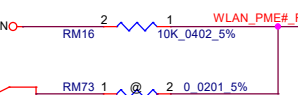
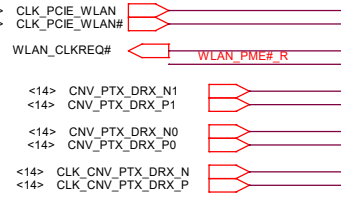
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLK_N1	73
70	UM_Power_SRC/GPIO/PEWake1#	RESERVED/REFCLK_P1	71
68	UM_Power_SRC/CLKREQ1#	GND	69
66	UM_SWAP/PERST1#	Reserved/PER1	67
64	RESERVED	Reserved/PER1	65
62	ALERT# (IO/3.3)	Reserved/PET1	61
60	I2C CLK (IO/3.3)	Reserved/PET1	59
58	I2C DATA (IO/3.3)	Reserved/PET1	57
56	WL_DISABLE1# (IO/3.3V)	Reserved/PET1	55
54	Reserved/W_DISABLE2# (IO/3.3V)	Reserved/PET1	53
52	PERST0# (IO/3.3V)	GND	51
50	SUSCLK(32KHz) (IO/3.3V)	REFCLK_N0	49
48	COEX1 (IO/1.8V)	REFCLK_P0	47
46	COEX2 (IO/1.8V)	GND	45
44	COEX3 (IO/1.8V)	PER1#	43
42	VENDOR DEFINED	PER1#	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	GND	37
36	UART RTS (IO/1.8V)	PET1#	35
34	UART CTS (IO/1.8V)	PET1#	33
32	UART TX (IO/1.8V)	GND	31
22	UART RX (IO/1.8V)	SDIO Resistor (IO/1.8V)	23
20	UART Wakeup (IO/3.3V)	SDIO Wakeup (IO/2.5V)	21
18	GND	SDIO DAT7N (IO/1.8V)	19
16	LED2 (IO/0.0)	SDIO DAT7P (IO/1.8V)	17
14	PCM_OUT/125 SQ_OUT (IO/1.8V)	SDIO DAT7 (IO/1.8V)	15
12	PCM_IN/125 SQ_IN (IO/1.8V)	SDIO DAT6 (IO/1.8V)	13
10	PCM_SYNC/125 WS (IO/1.8V)	SDIO CMD0 (IO/1.8V)	11
8	PCM_CLK/125 SCK (IO/1.8V)	SDIO CLK (IO/1.8V)	9
6	LED1 (IO/0.0)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1



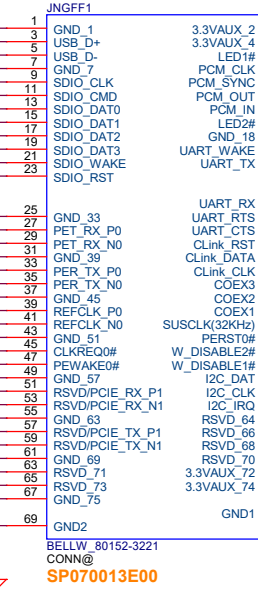
(For BT)



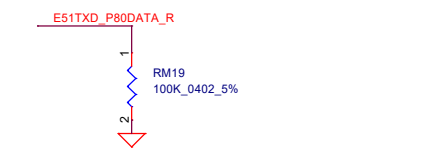
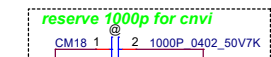
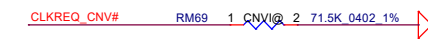
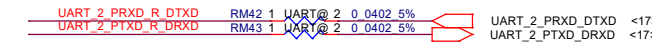
(From PCH CLKOUT2)
PCIE CLK



KEY E



Co-layout with CNVi for SW debug



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								M.2 Key E (WLAN)			
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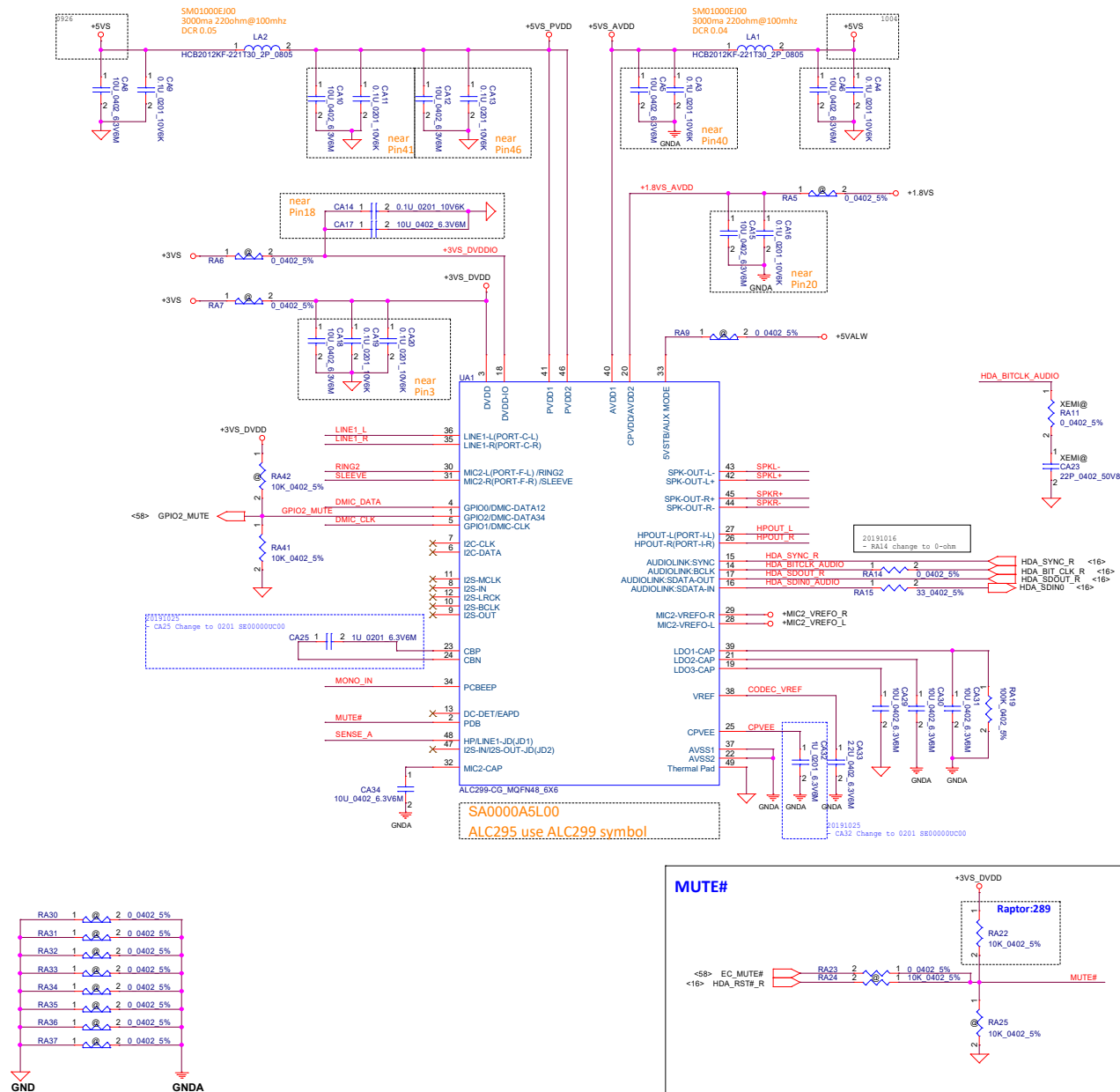
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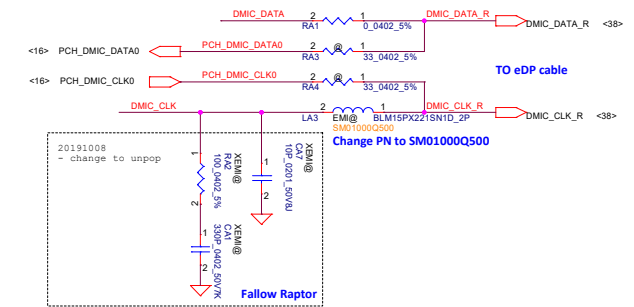
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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				GH51G M/B LA-L181P	1A
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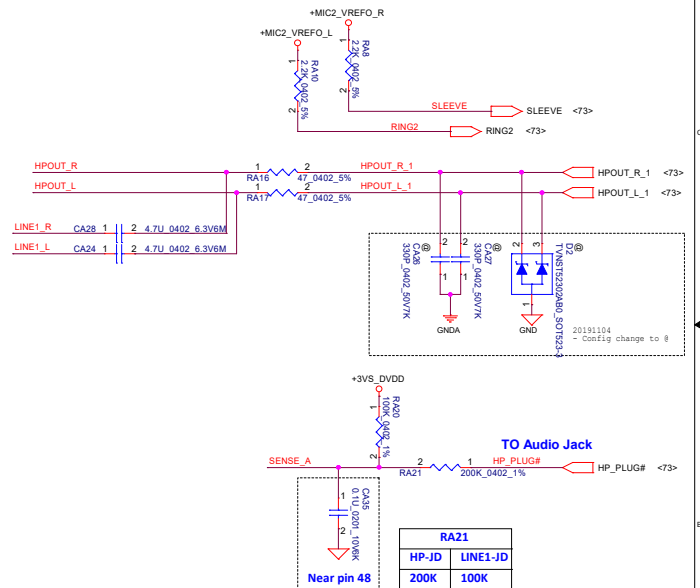
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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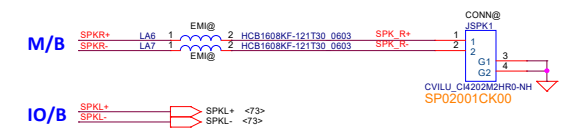
Digital MIC



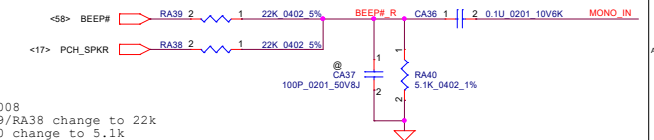
Headphone Out



Speaker



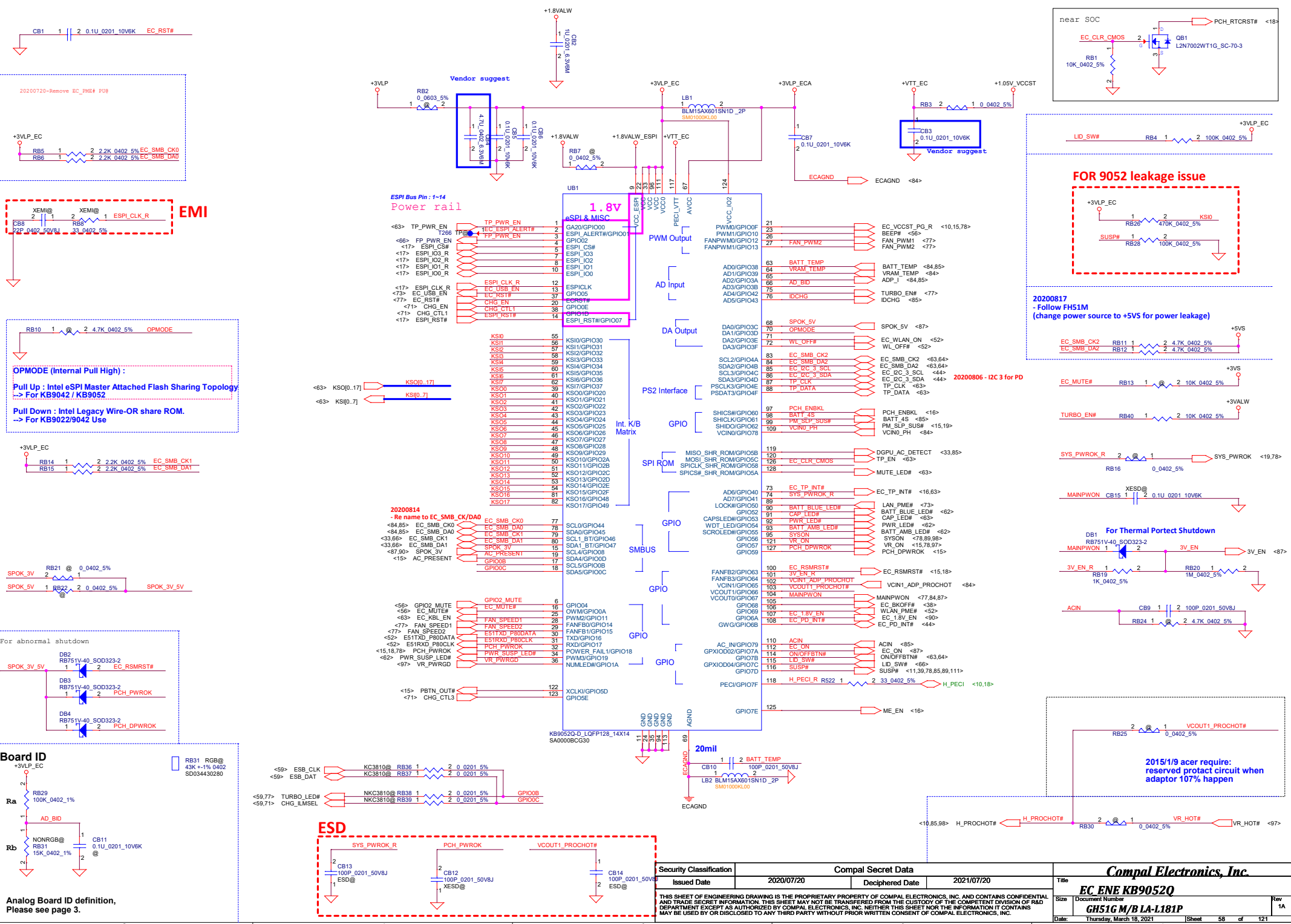
BEEP



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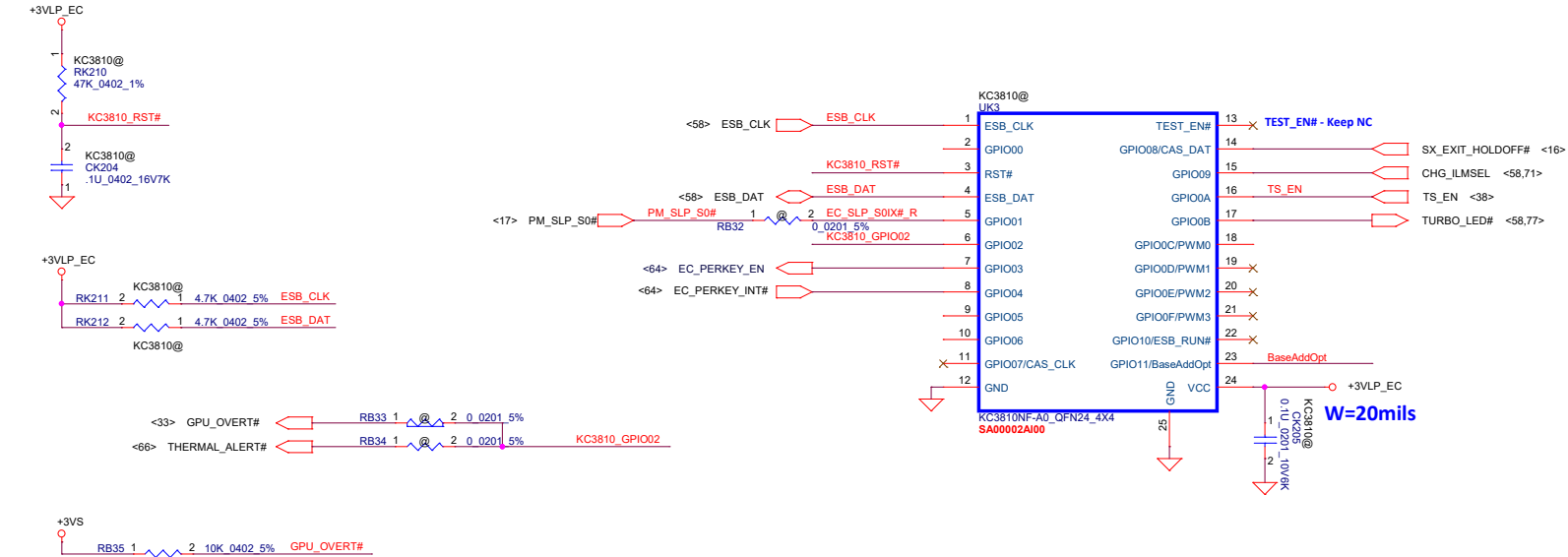
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OMEN New ESB CLK&DAT for Extend I/O

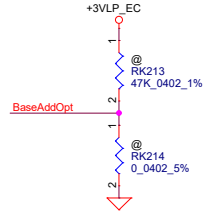
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.



Need EC confirm

[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and
the other keep NC or initial High

- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08



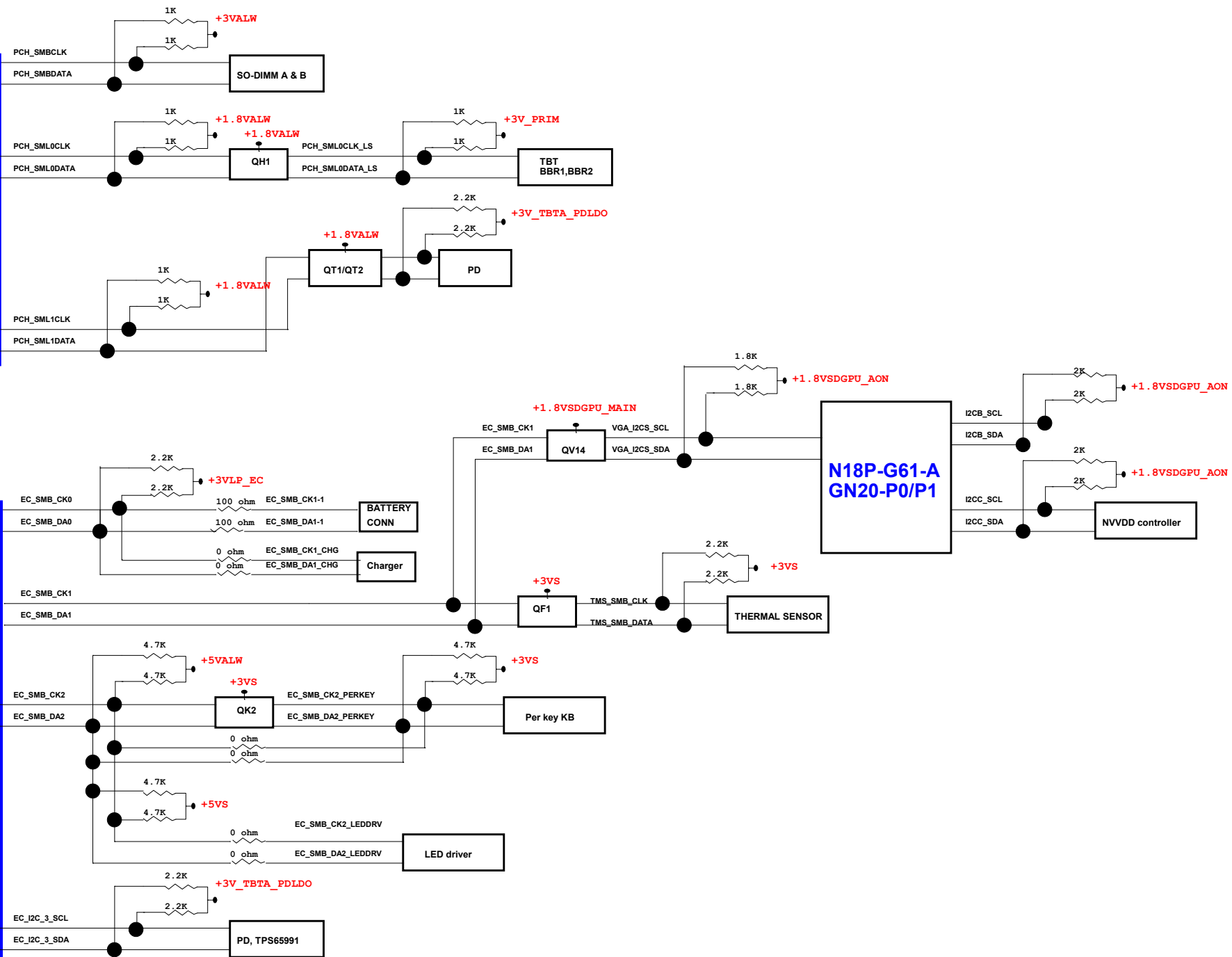
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Issued Date	2020/07/20	Deciphered Date	2021/07/20	Title	Extend I/O KC3810
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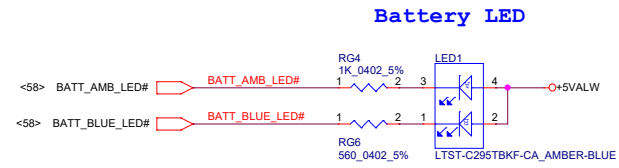
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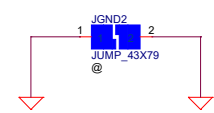
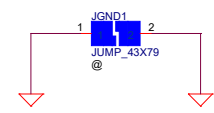
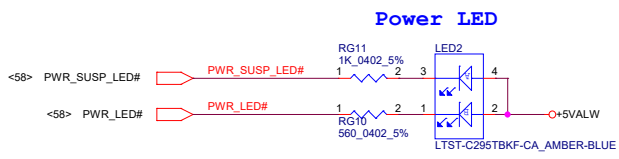
TigerLake
PCH - H

KB9052



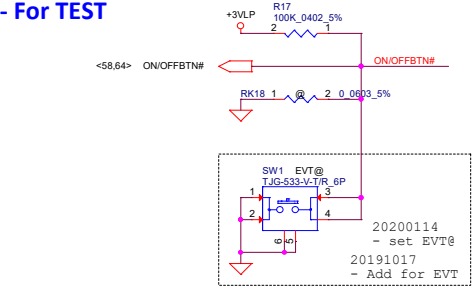


20200211
- RG4/RG11 change to 1k

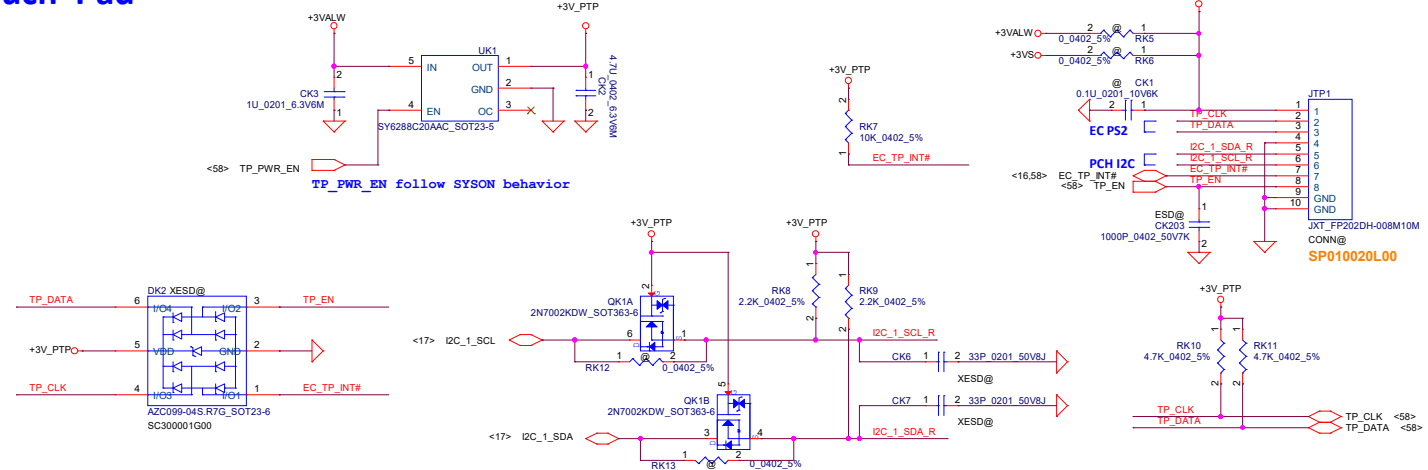


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ON/OFF BTN
- For TEST



Touch Pad

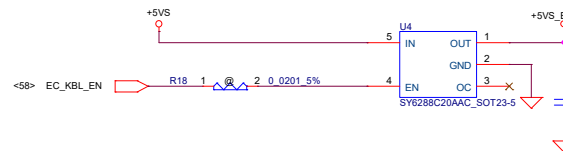


LED driver

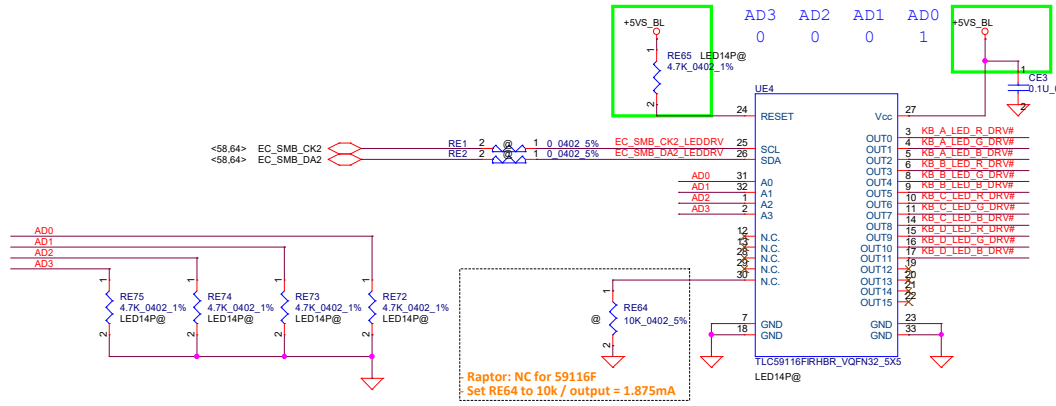
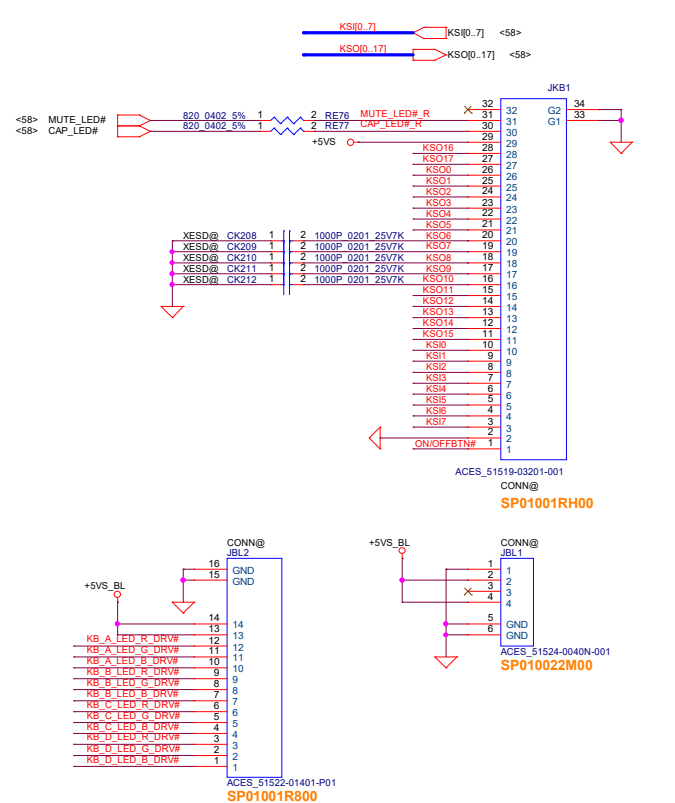
20191016
- Remove QE62/RE70/RE69
- PU +5VALW @ EC

20191001
- Change to +5VS only
- KBL_EN only (Check EC Code)
- pop (Normal & RGB)

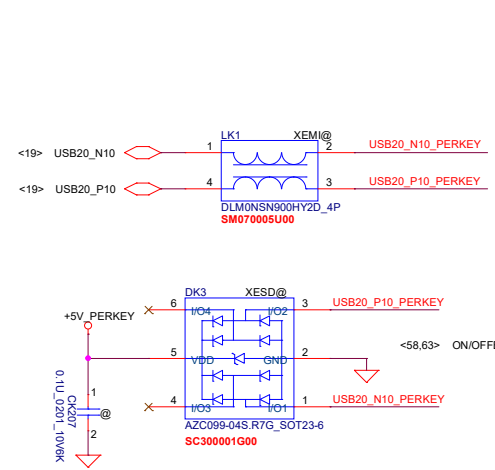
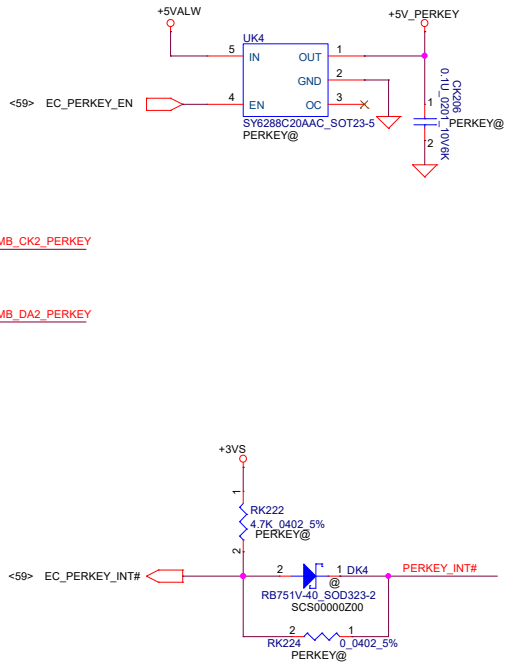
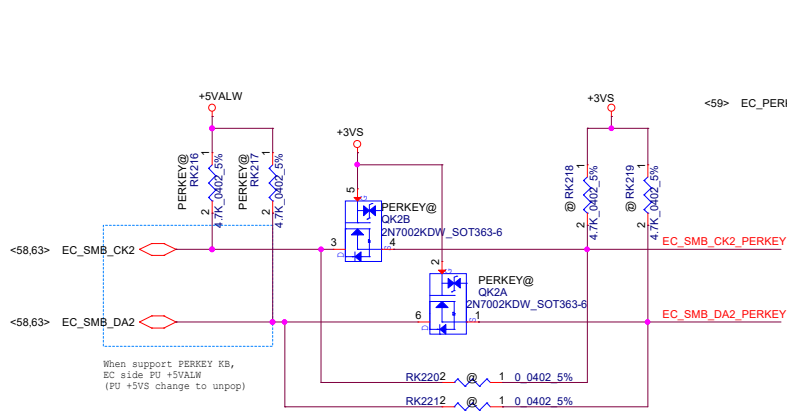
20200115
- R41/R18 change to R-short



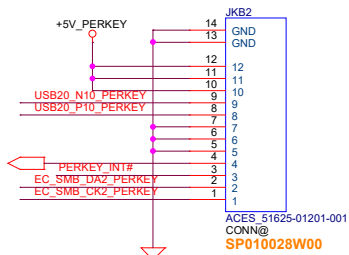
KB Conn. / Backlight



Raptor: NC for 59116F
Set RE64 to 10k / output = 1.875mA



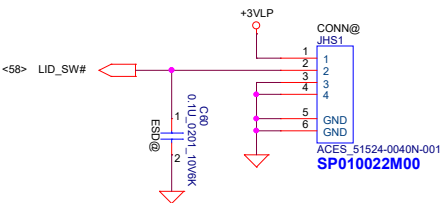
Per Key Conn.



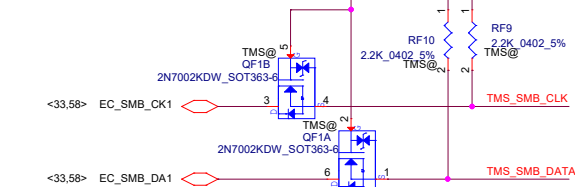
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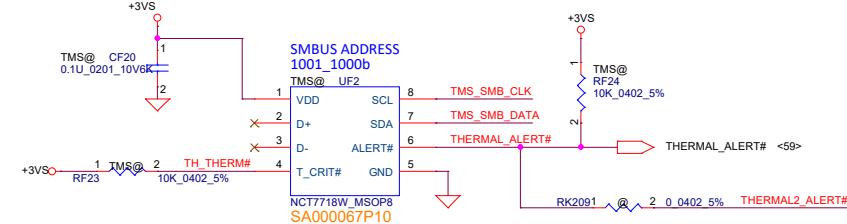
To Hall sensor/B



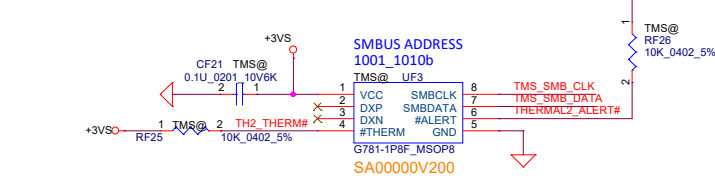
THERMAL SENSOR



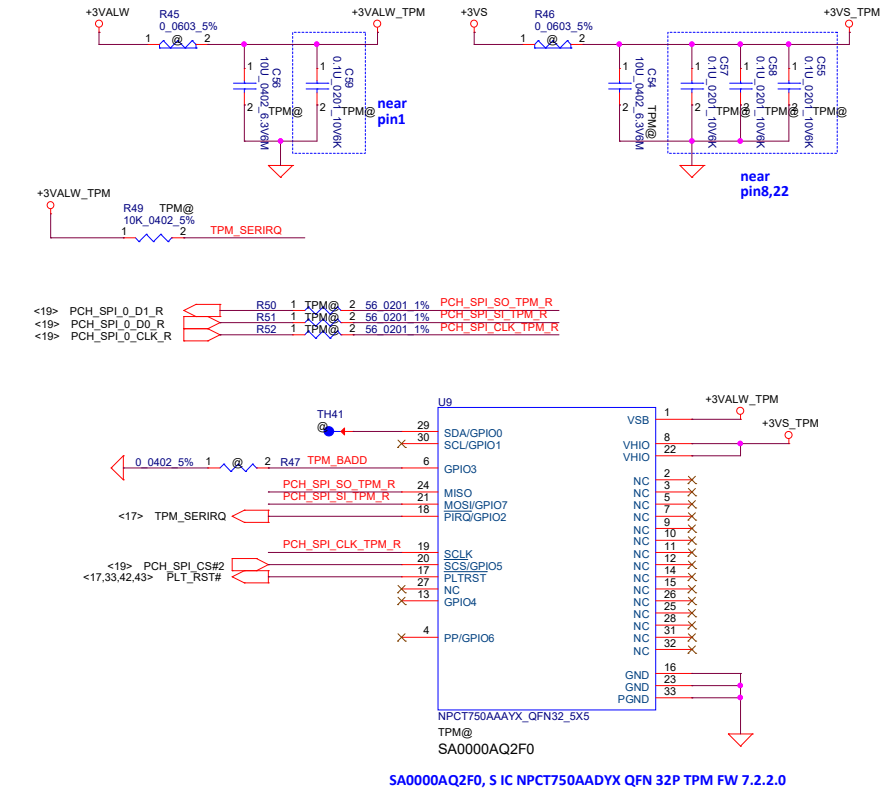
Close to SO-DIMM



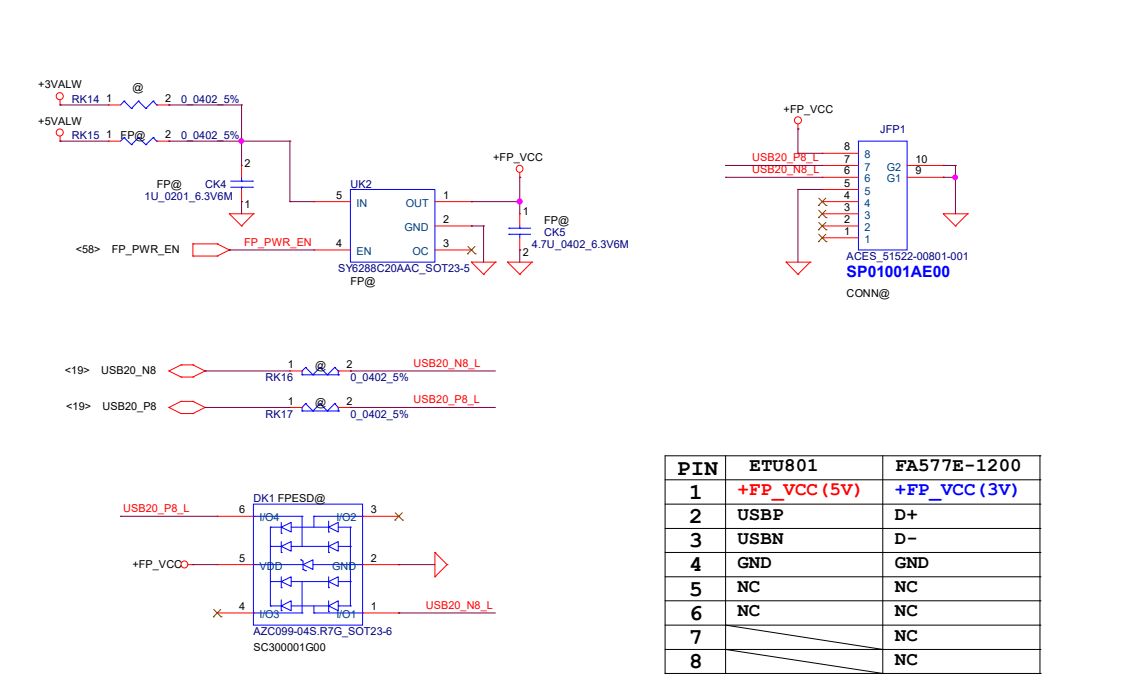
Close to Thermal SKIN



TPM



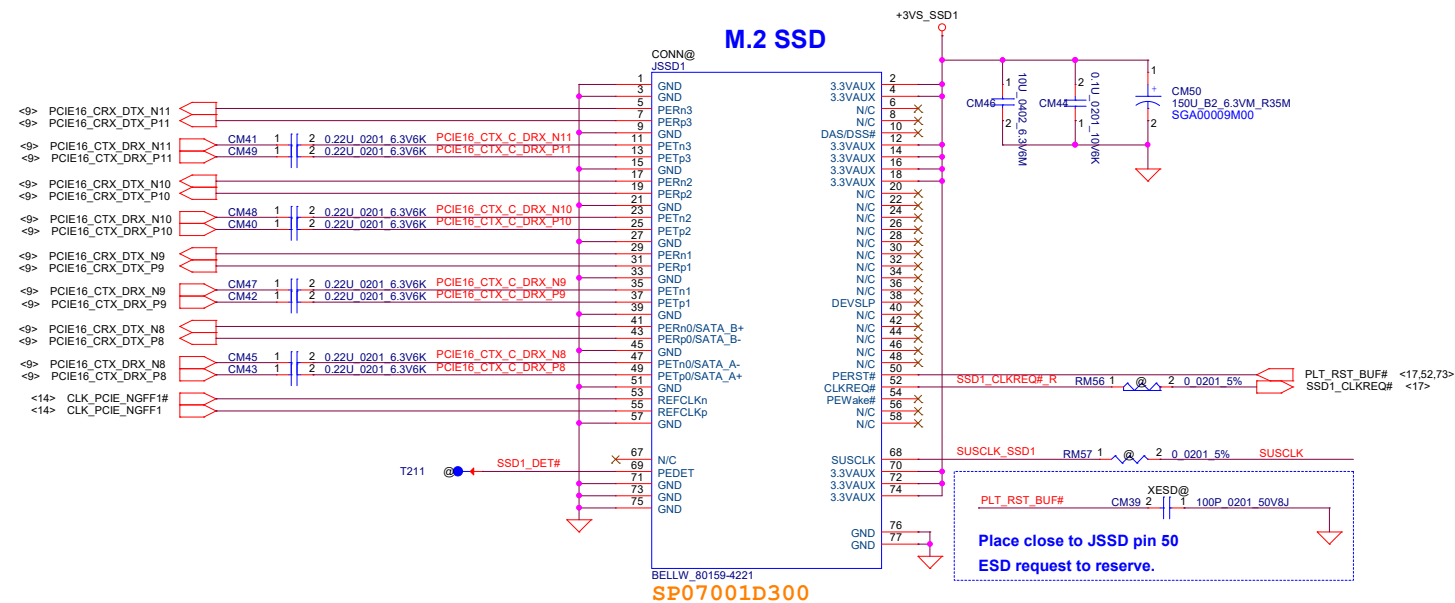
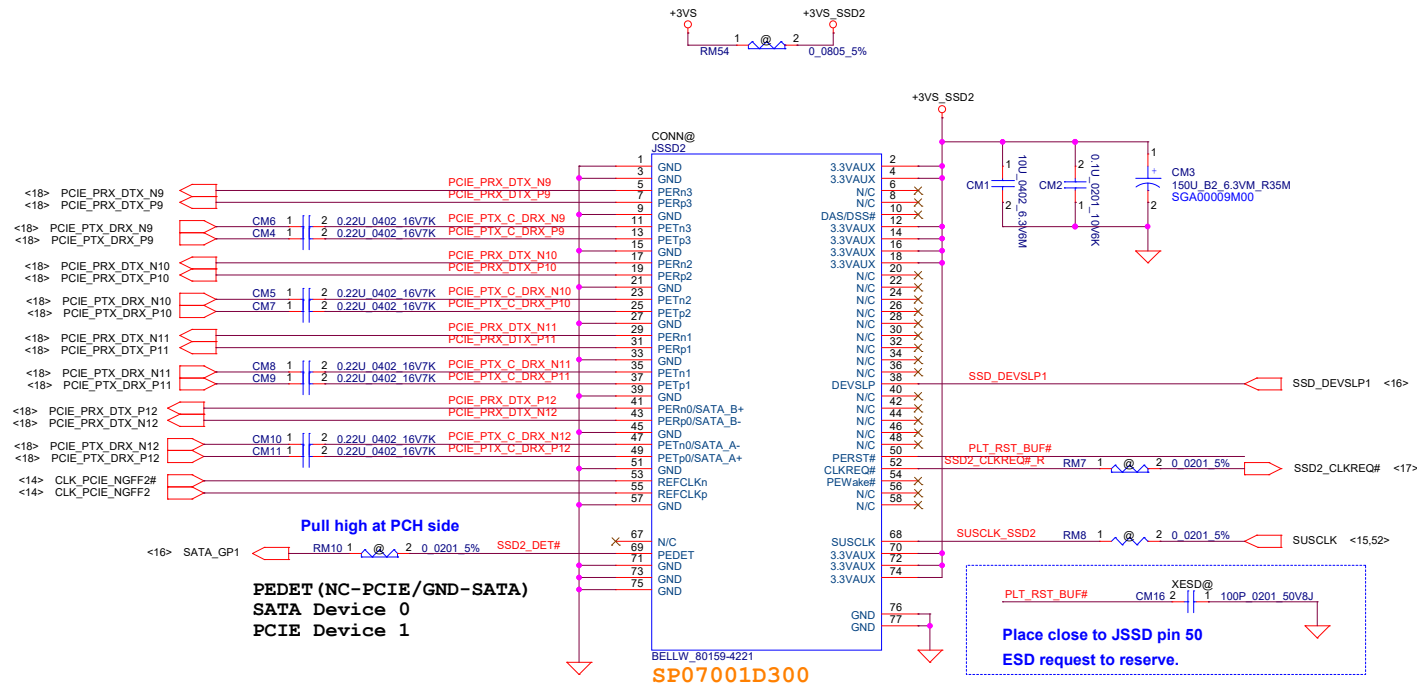
Finger Print



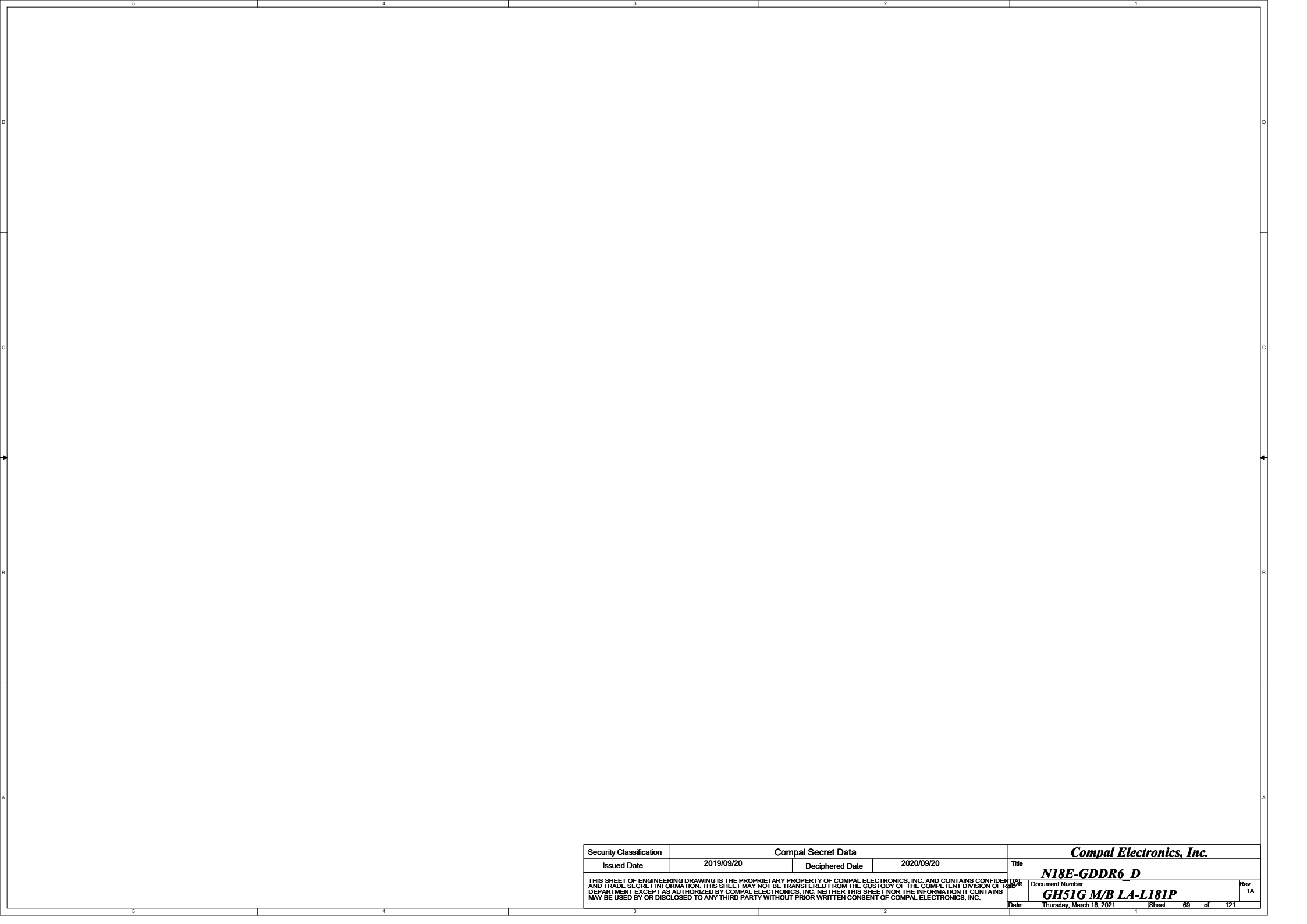
PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC



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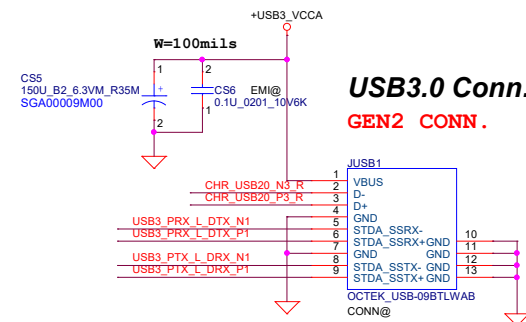
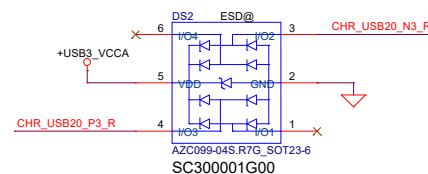
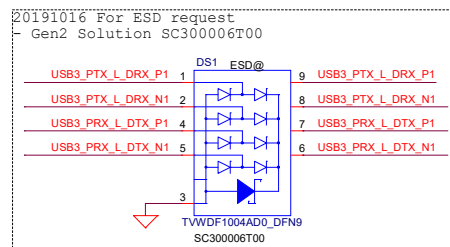
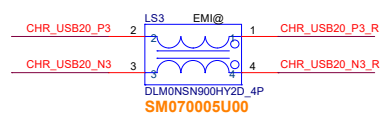
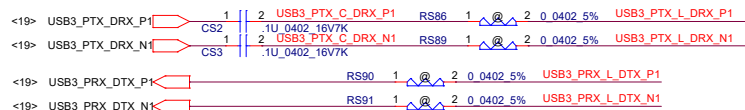


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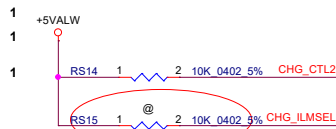
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USB3.0



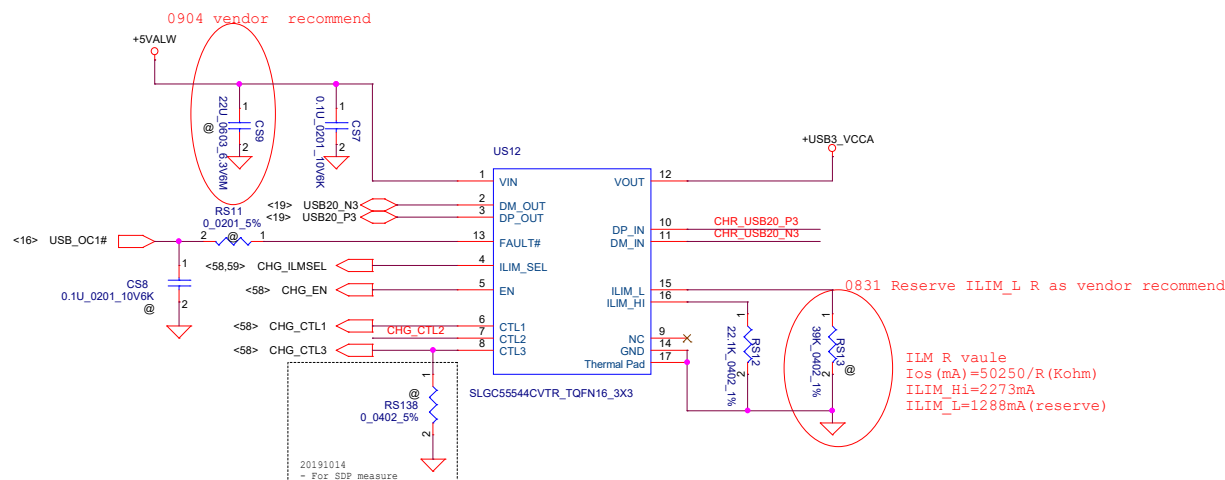
USB Host Charger



0911 Rerserve PU, vendor suggest to EC control
if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
	1	1	1	1	CDP	ILIM_H	Data Lines Connected

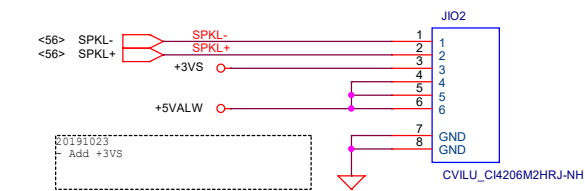
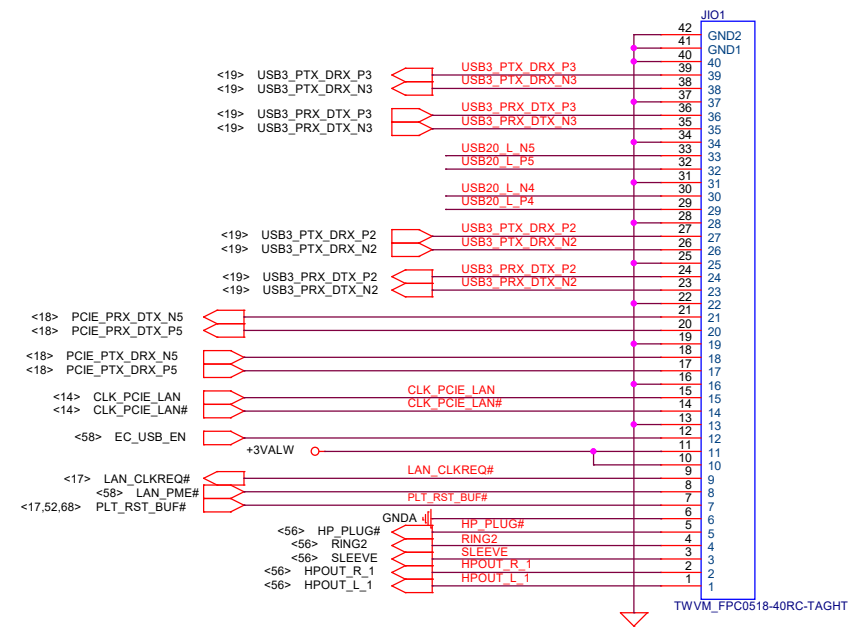
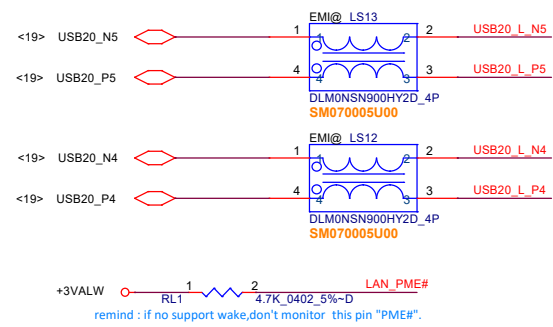


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20190918
USB3 Port3 move to IO/B

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IO/B CONN



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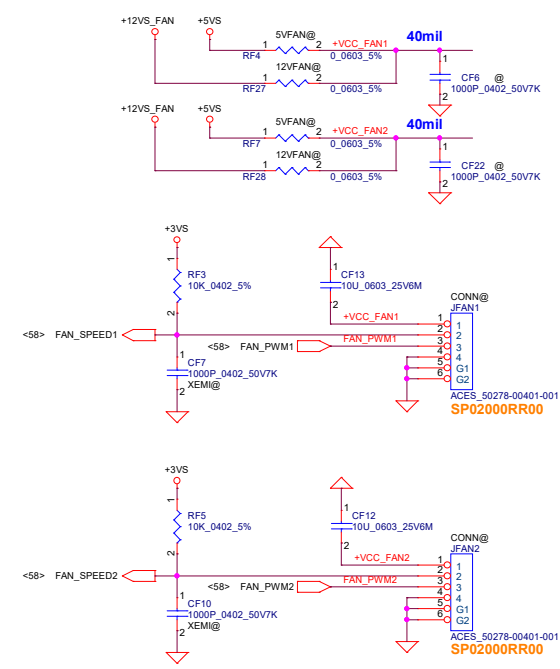
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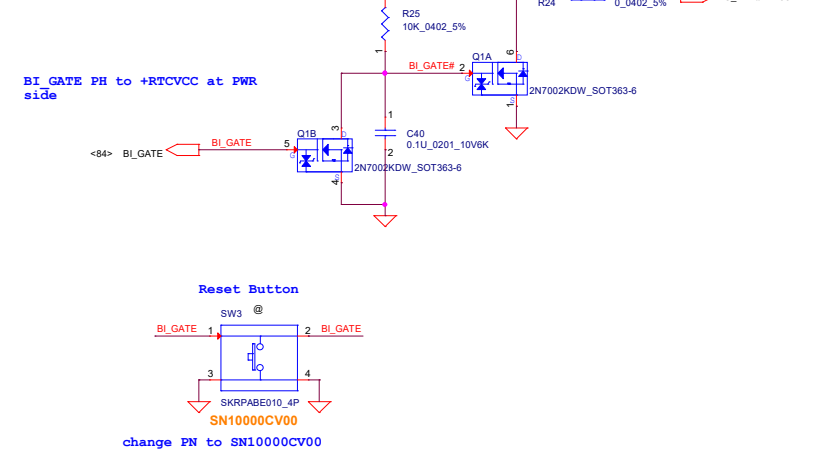
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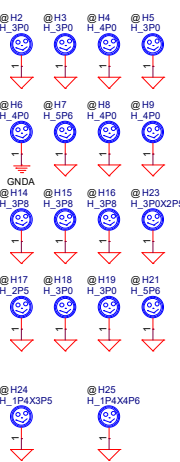
FAN Conn



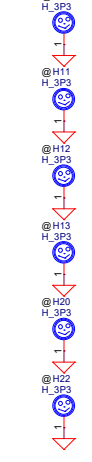
Reset Circuit



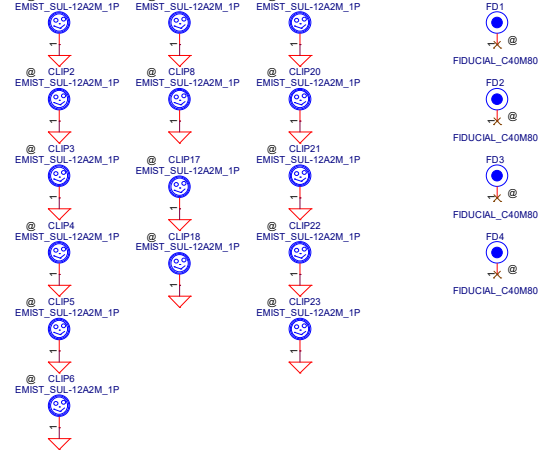
Screw Hole



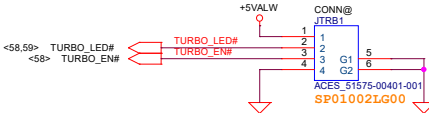
Stand OFF



Clips

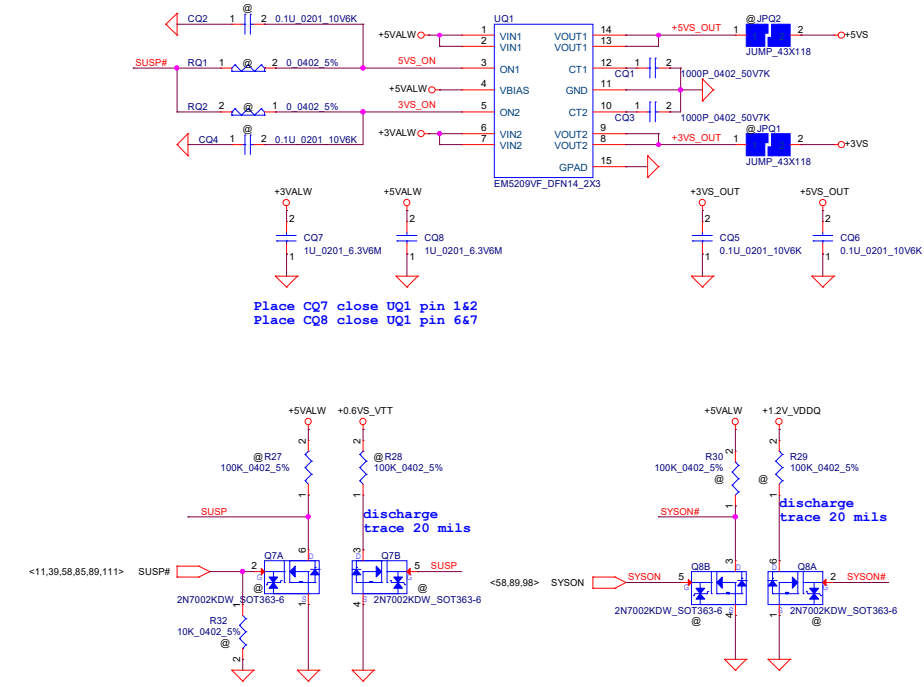


Turbo Key

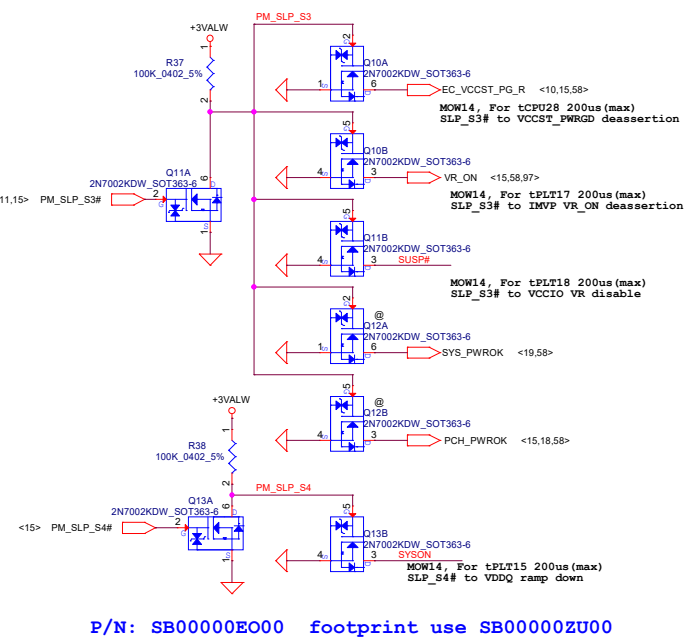


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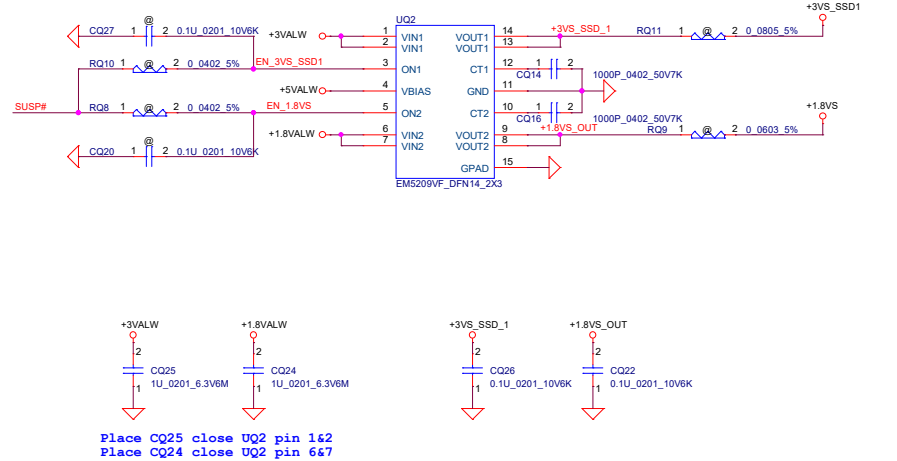
System DC interface



For Power ON/Off Sequence



+1.8VALW TO +1.8VS / +3VALW TO +3VS_SSD1



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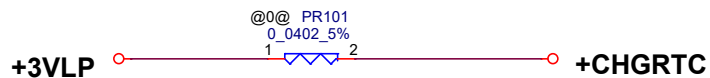
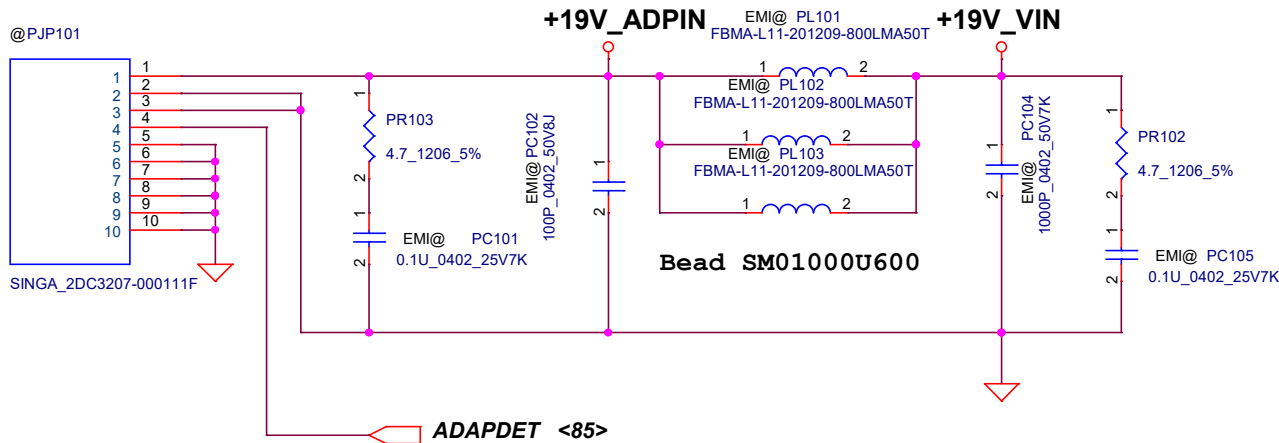
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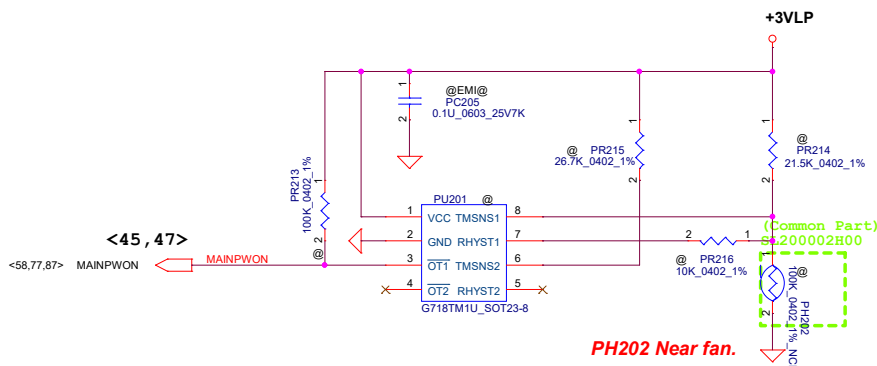
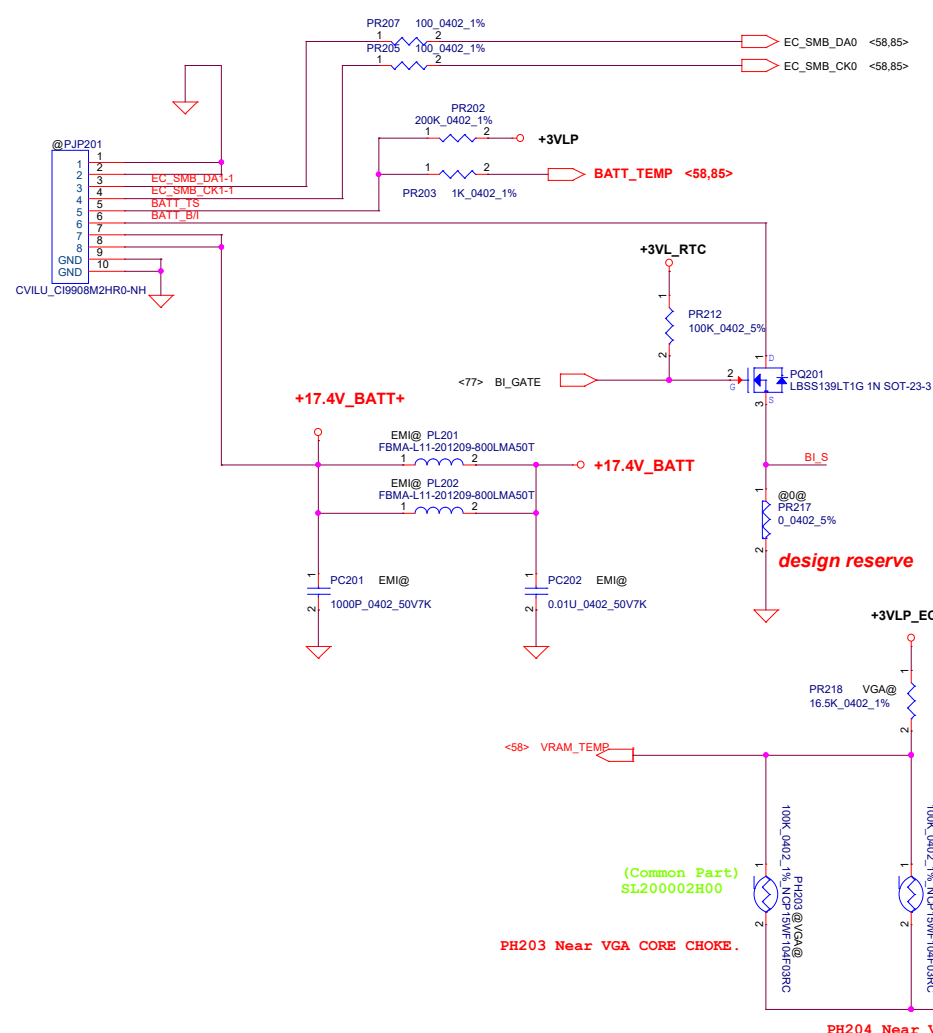
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Battery Bot Side

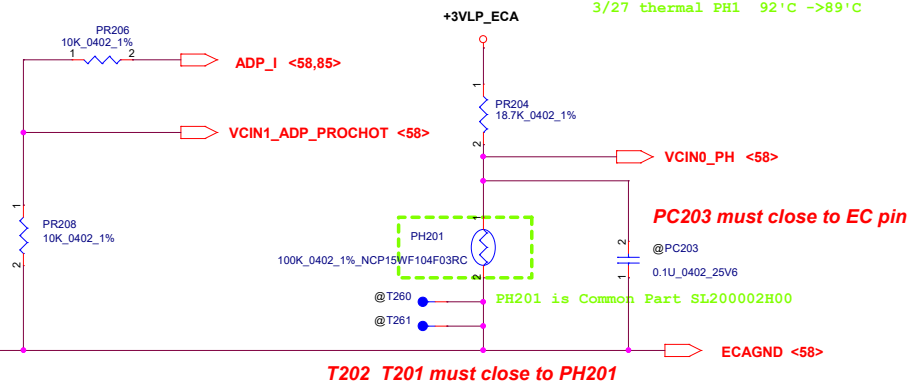
- PIN1 GND
- PIN2 GND
- PIN3 SMD
- PIN4 SMC
- PIN5 TEMP
- PIN6 BI
- PIN7 Batt+
- PIN8 Batt+



When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	89'C, 1V	56'C, 2V
PH202 (ohm)	8.0524K	26.11K

3/27 thermal PH1 92'C ->89'C



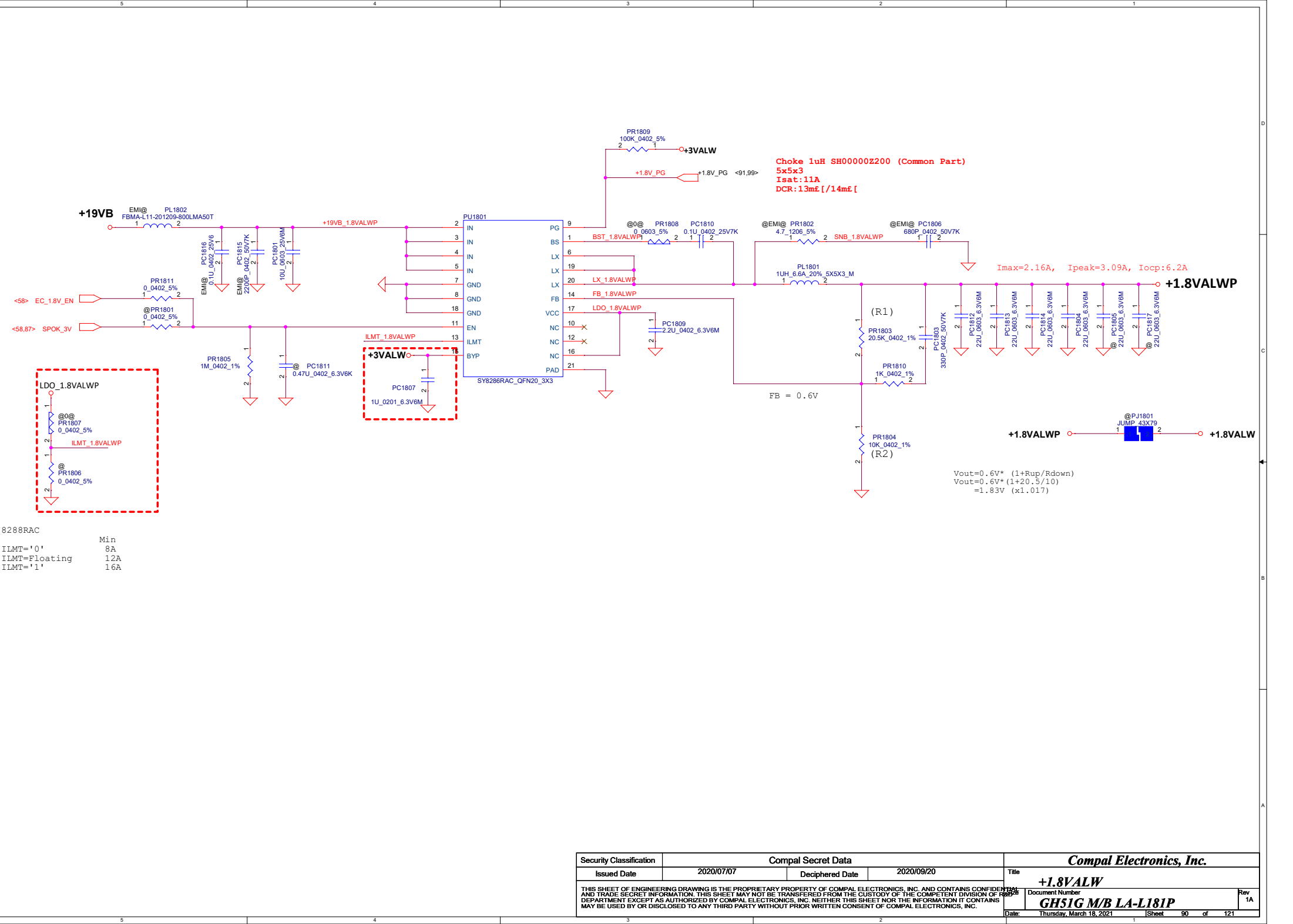
$$ADP\ I=20*I(adapter)*0.01$$
$$I(adapter)=adapter\ (W)*130\%/19$$

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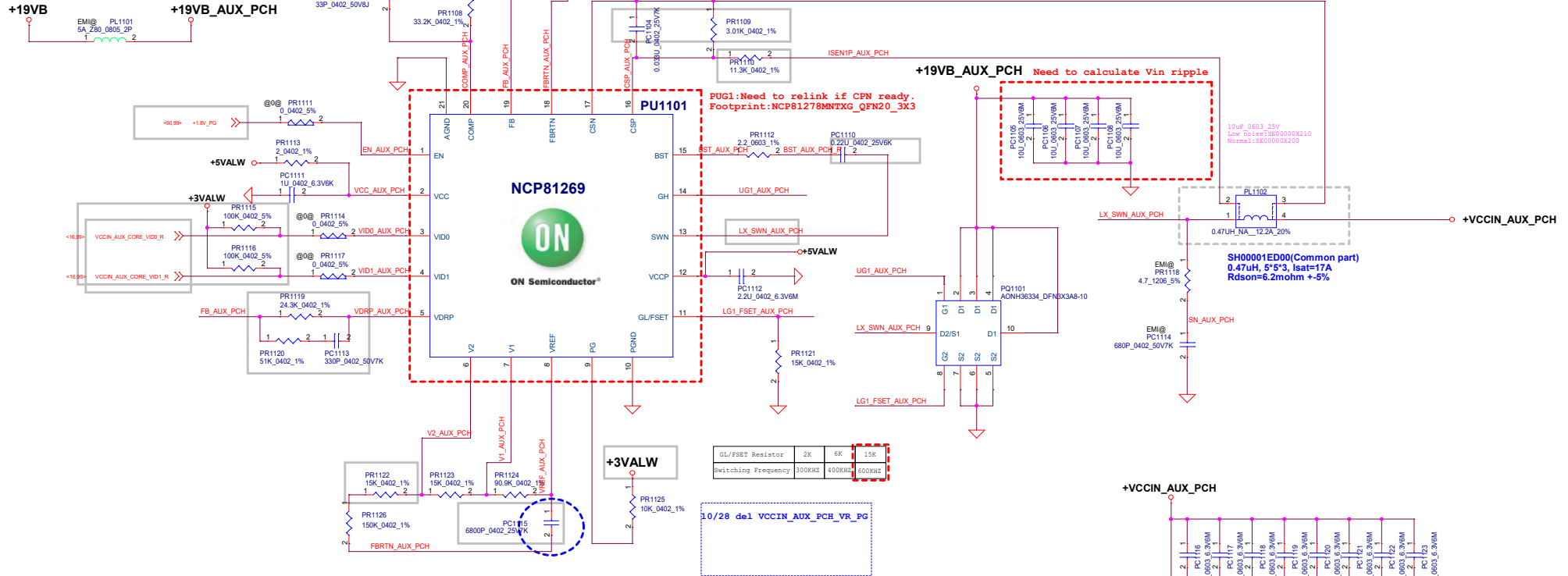
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VCCIN_AUX_VID

VID[1] Pin State	VID[0] Pin State	VCCIN_AUX Voltage (V)	Usage
0	0	0	Power Saving State
0	1	1.1	Power Saving State
1	0	1.65	Unused
1	1	1.8	Initial boot and full current operation



TGL-H 8+1 45W, baseline VCCIN_AUX
Peak Current 35A (ICCmax)
to CPU=26.5A
to PCH=8.5A
TDC :18A
to CPU=A
to PCH=A
DC Load line : 1.5mohm
AC Load line : 3.5mohm
Current limit : 69A(min) by IC pin. setting (per phase)
Fsw=600kHz

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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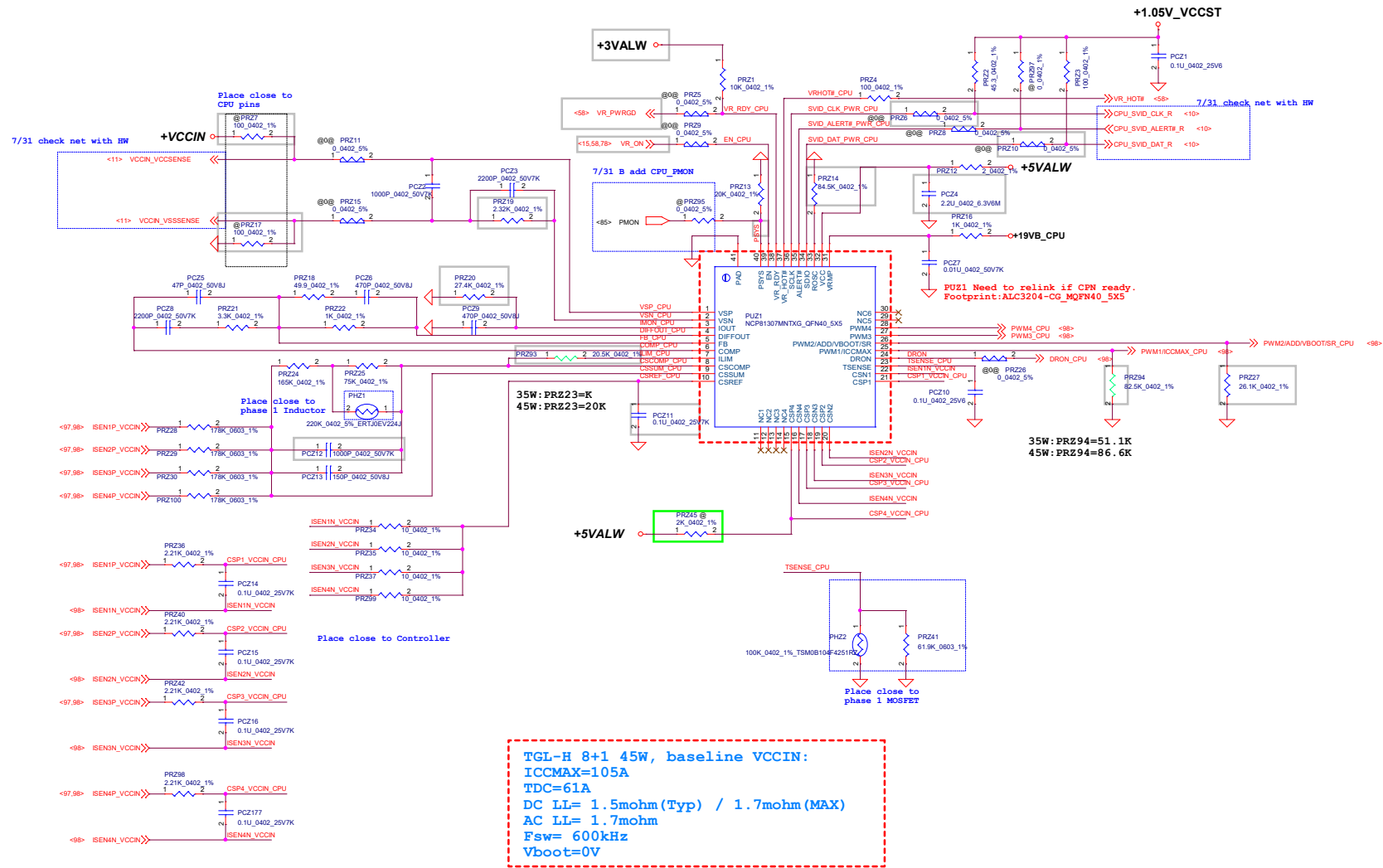
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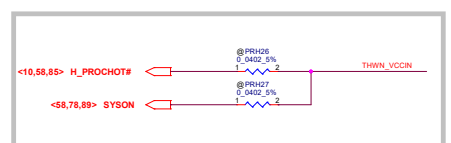
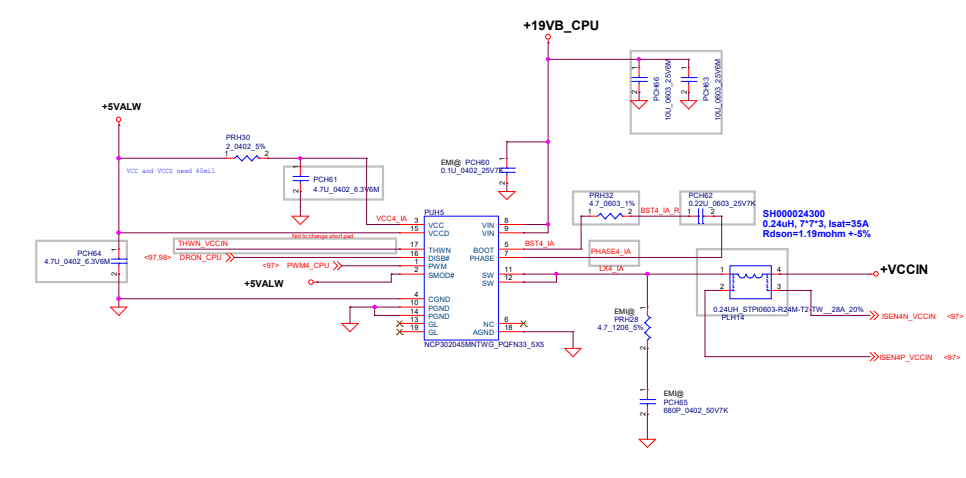
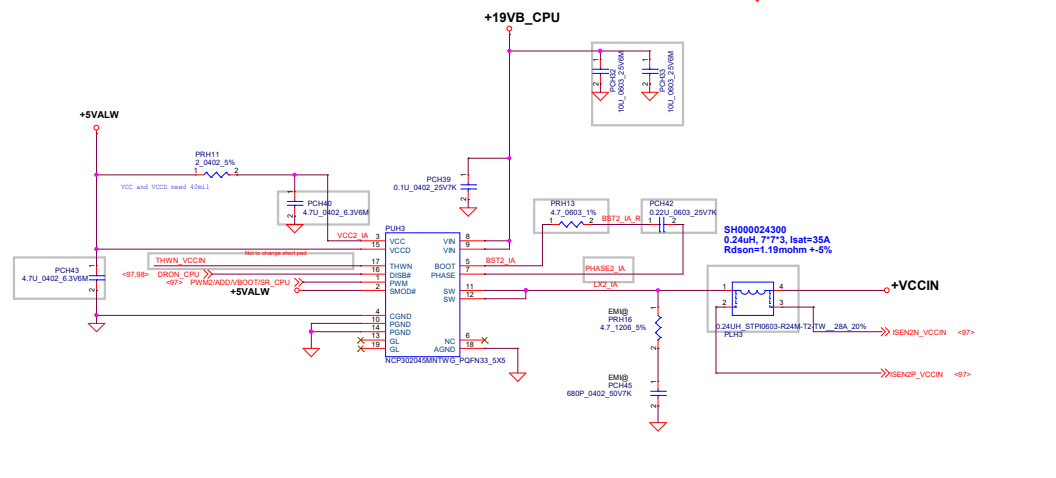
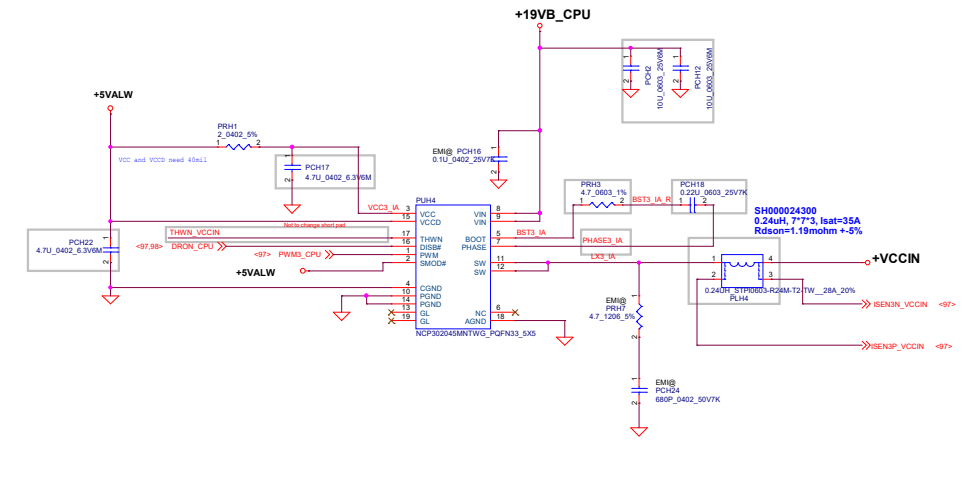
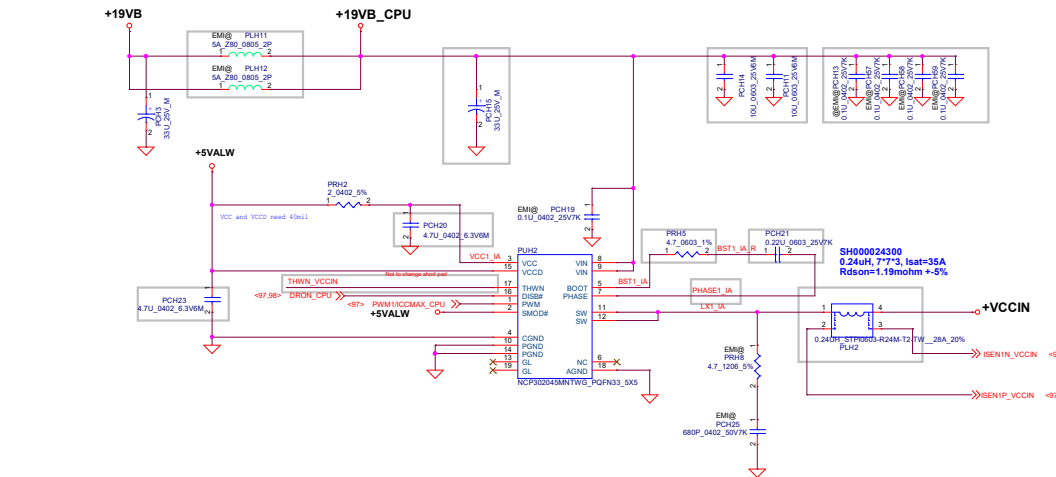
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				+VCC GT/+VCC SA
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+VCCIN

12

10

11

10

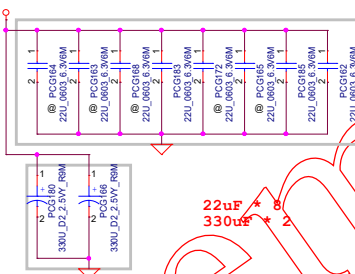
22uF * 23
22uF * 20 Placeholder

330uF * 3
220uF * 1

AUX Decoupling Cap

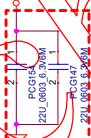
CPU Primary Side

+VCCIN_AUX



22uF * 8
330uF * 2

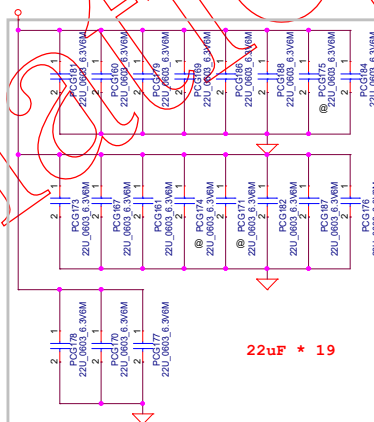
+VCCIN_AUX



Place near to VRM

CPU Secondary side

+VCCIN_AUX



22uF * 19

Follow Intel PDG Rev0.8 excel (618429)
+VCCIN Output CAP :

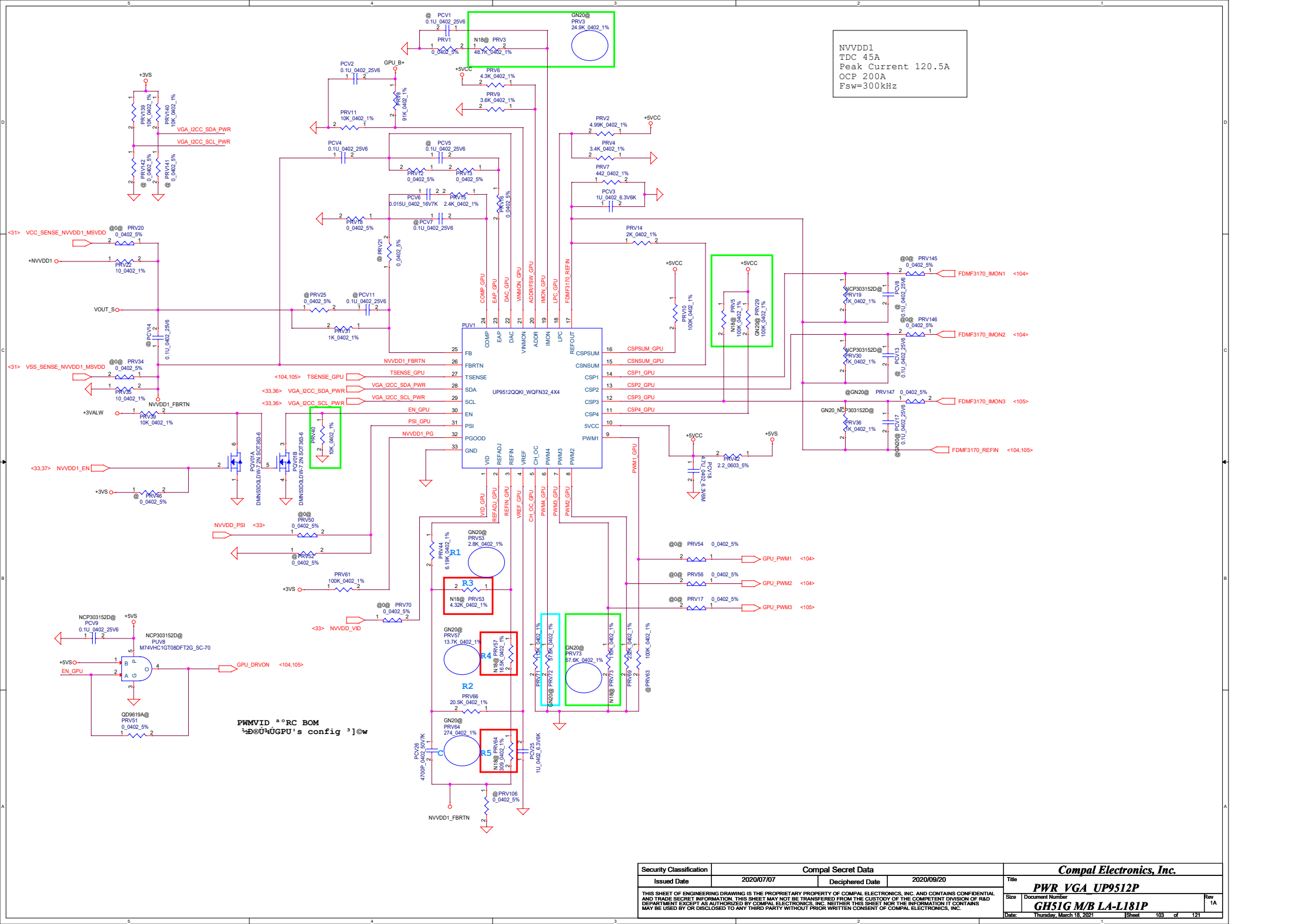
CPU Primary Side:
330uF B2 *2 pcs
47uF 0603 *4 pcs
12pF *6 for FIVR solution

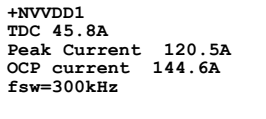
CPU Secondary side:
10uF 0402 *6 pcs
47uF 0603 *8 pcs

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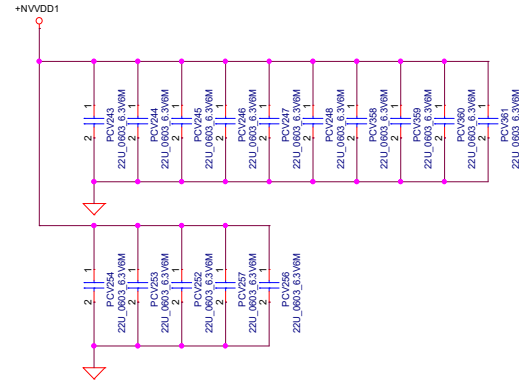
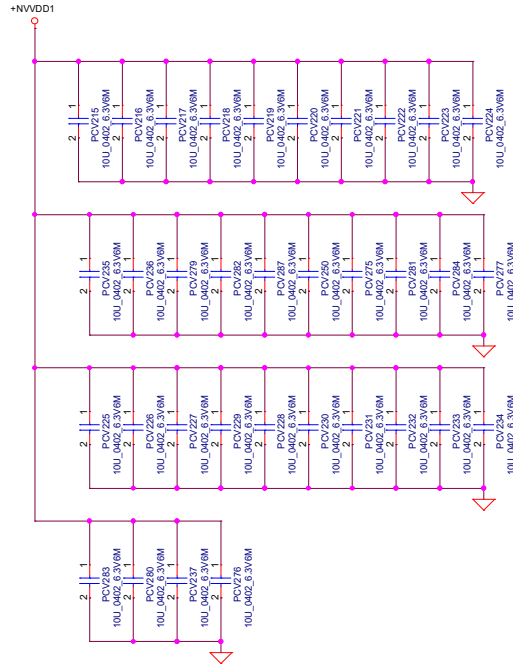
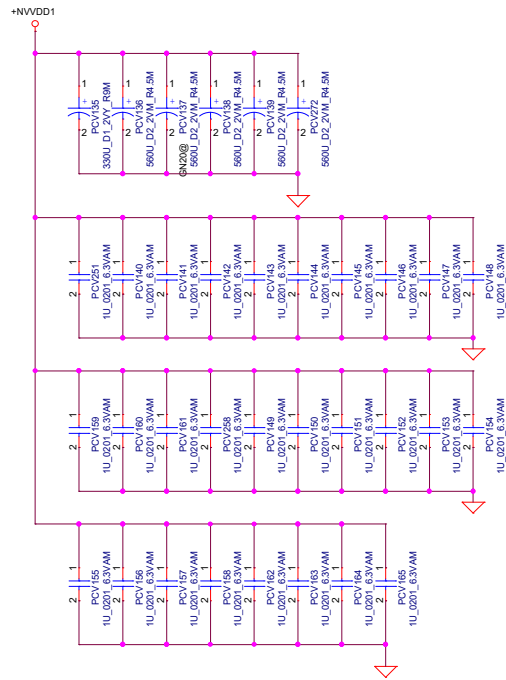


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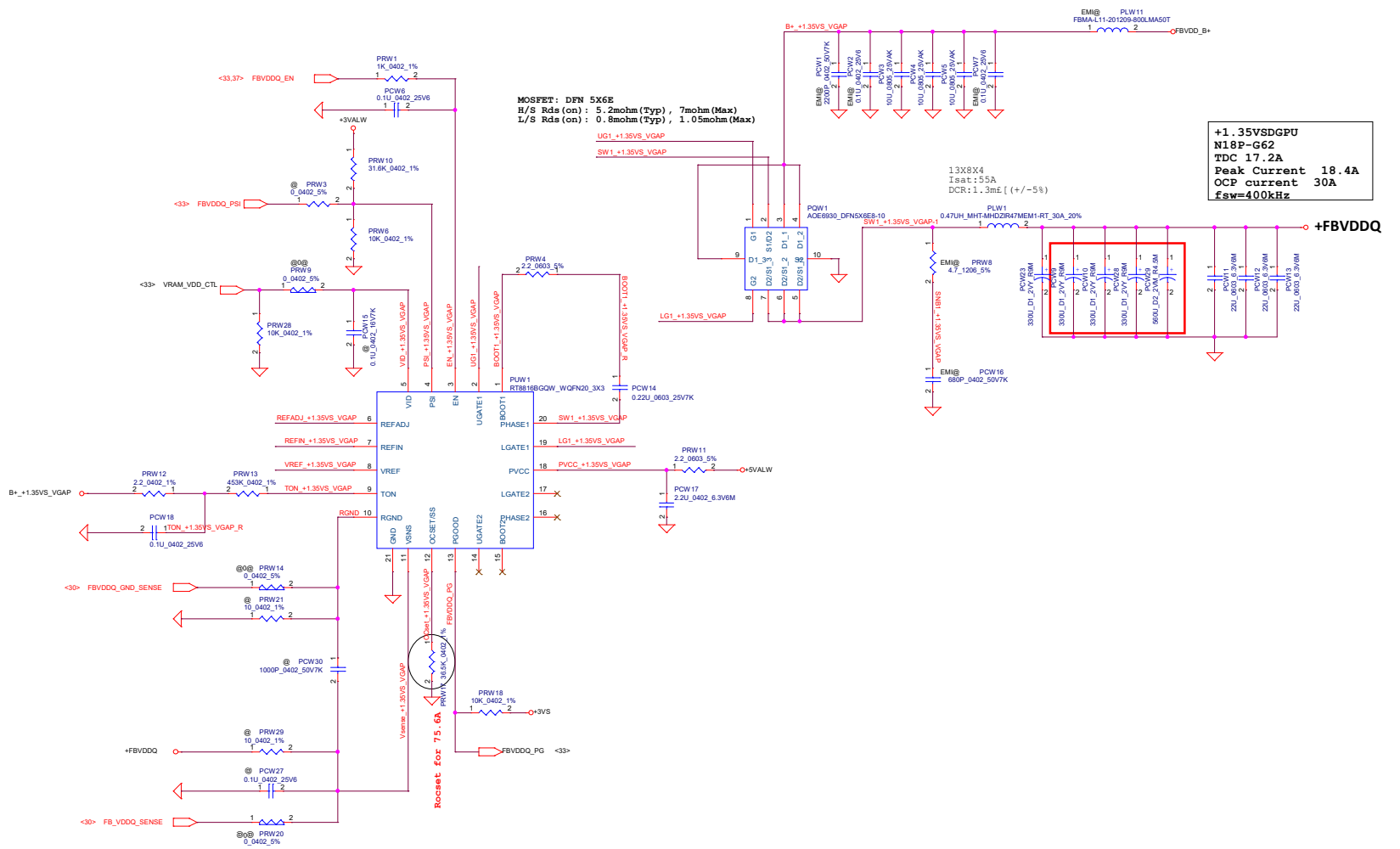
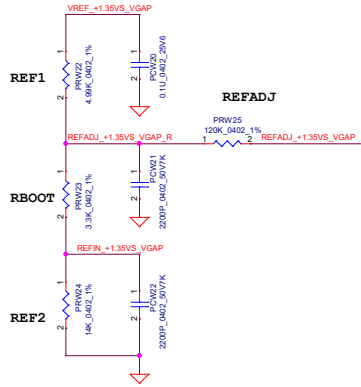
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+NVVDD
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28



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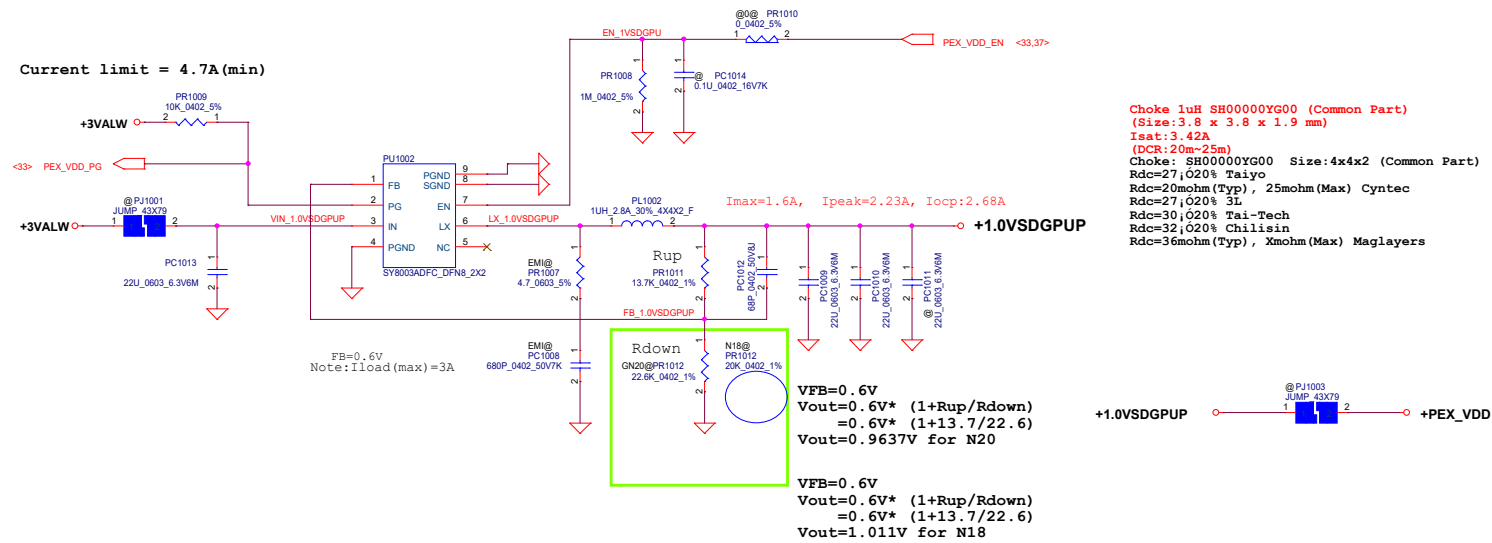
Samsung & Micron VRAM
When, VRAM VDD_CTL=High
Vboot=1.25V
When, VRAM VDD_CTL=Low
Vboot=1.2V



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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	NA	NA	P97	PUZ1 change from NCP81307M_SA0000DOH10 to NCP81307M_SA0000DOH00	0126	EVT2
02	NA	material shortage	P98,P99	PLG101,PLH2,PLH3,PLH4,PLH14 change from 0.24u_7x7x3_SH00000RE00 to 0.24u_7x7x3_SH000024300	0126	EVT2
03	NA	CPU transient	P97	PRZ19 change from 1.65k_0402_SD034165180 to 2.32k_0402_SD00000WS80 PRZ20 change from 26.7k_0402_SD034267280 to 27.4k_0402_SD034274280 PCZ13 change from 39pF_0402_SE071390J80 to 150pF_0402_SE071151J80 PCZ11 change from 0.22u_0402_SE00001MT00 to 0.1u_0402_SE00000W210	0126	EVT2
04	NA	CPU transient	P99	PRG107 change from 3.48k_0402_SD034348180 to 4.02k_0402_SD034402180 PRG108 change from 4.75k_0402_SD034475180 to 5.49k_0402_SD034549180	0126	EVT2
05	NA	NA	P99	PRG126 & PRG127 100k_0402_SD028100380 change to reserve	0126	EVT2
06	NA	material shortage	P97	PCZ4 change from 2.2uF_0402_SE000013H00 to 2.2uF_0402_SE000008880	0126	EVT2
08	NA	material shortage	P99	PCG150 change from 0.1u_0402_SE00000G800 to 0.1u_0402_SE00000G880	0126	EVT2
09	NA	material shortage	P91	PC1111 change from 1u_0402_SE000010V00 to 1u_0402_SE000000K80	0202	EVT2
10	NA	material shortage	P99	PCG149 change from 1u_0402_SE000010V00 to 1u_0402_SE000000K80	0202	EVT2
11	NA	material shortage	P101	PC1039,PC1040,PC1044,PCG166,PCG180 change from 330u_2.5V_SGA00002680 to 330u_2.5V_SGA0000E800	0202	EVT2
12	NA	reduce part count	P91	PR1104,PR1106,PR1111,PR1114,PR1117 change from 0_0402_SD028000080 to R-short	0208	PVT
13	NA	reduce part count	P97	PRZ5,PRZ6,PRZ8,PRZ9,PRZ10,PRZ11,PRZ15,PRZ26 change from 0_0402_SD028000080 to R-short	0208	PVT
14	NA	reduce part count	P99	PRG103,PRG105,PRG109,PRG112,PRG113 change from 0_0402_SD028000080 to R-short	0208	PVT

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